Implementation of a Power Efficient High Performance FPU for SCOORE

Presenter: Rigo Dicochea

Authors: W. Ashmawi, J. Burr, A. Sharma, J. Renau

MASC Research Lab

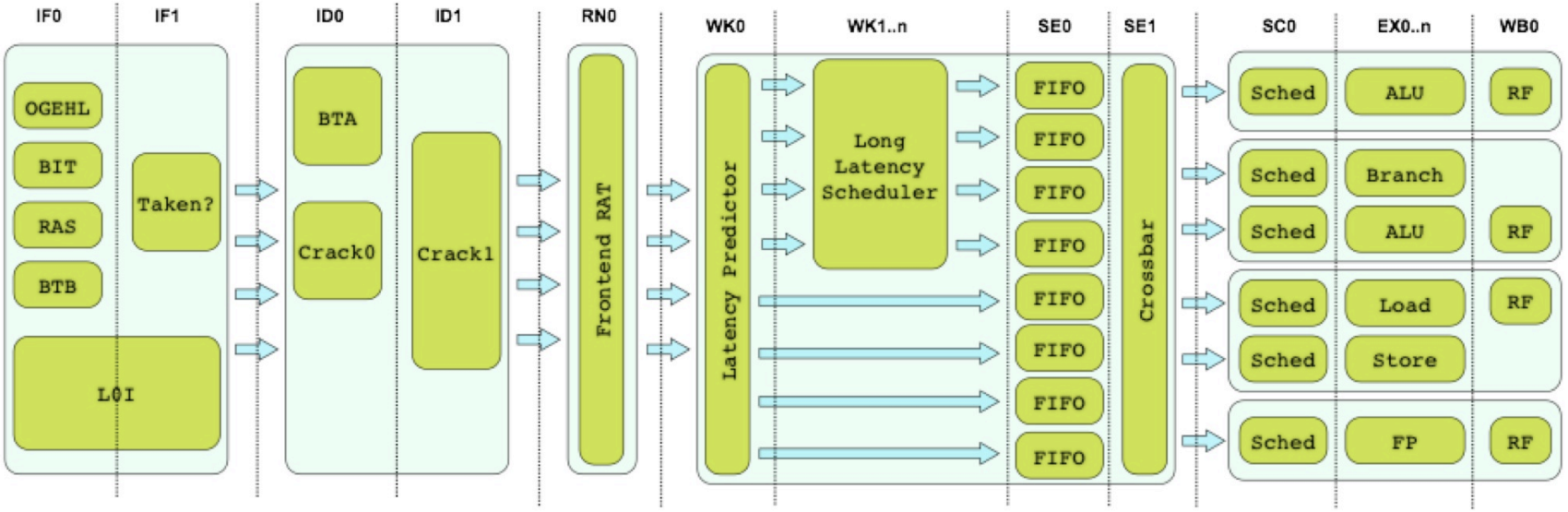
University of California, Santa Cruz

http://masc.soe.ucsc.edu/

SCOORE

- SPARC V8 ISA
- Out-Of-Order Execution
- 4-Issue Superscalar
- 12-Stage Pipeline

- 1.4 GHz 90nm ASIC
  - Frequency/Power Optimization
- 155 MHz FPGA
  - Area Minimization



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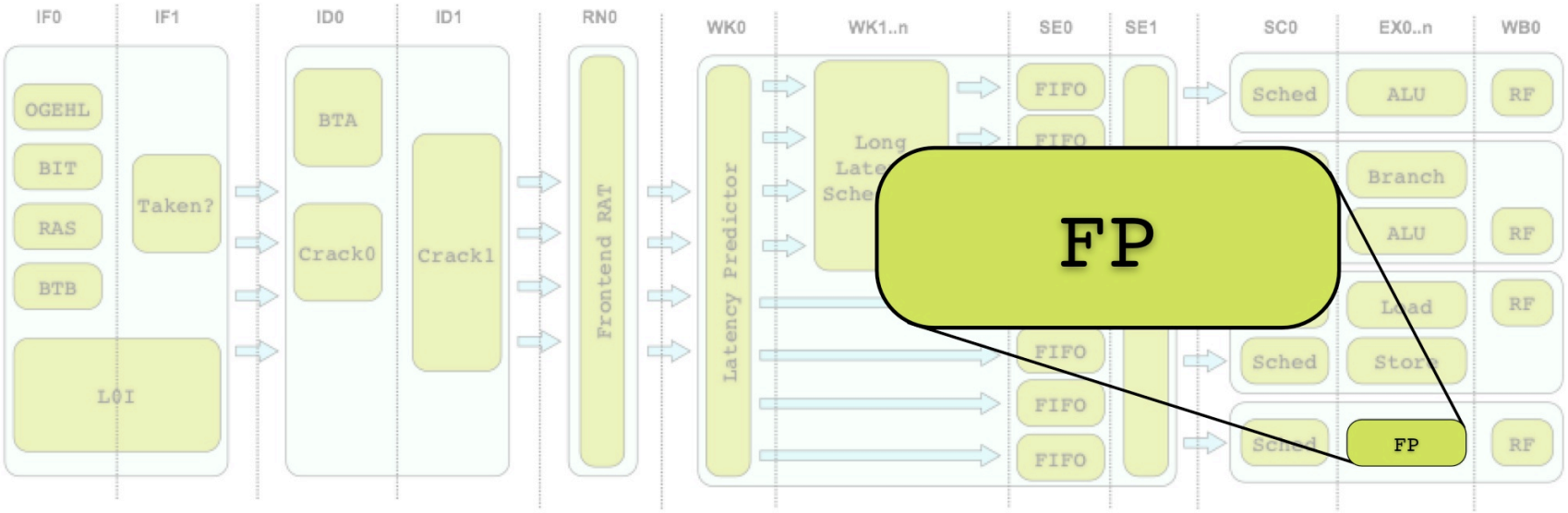


Outline

- Floating Point Unit Architecture
  - Pipeline Flow
- ASIC/FPGA Synthesis Results
- Power Optimization Methodology
  - Switching Activity
  - Clock Gating
- Conclusion

Floating Point Unit

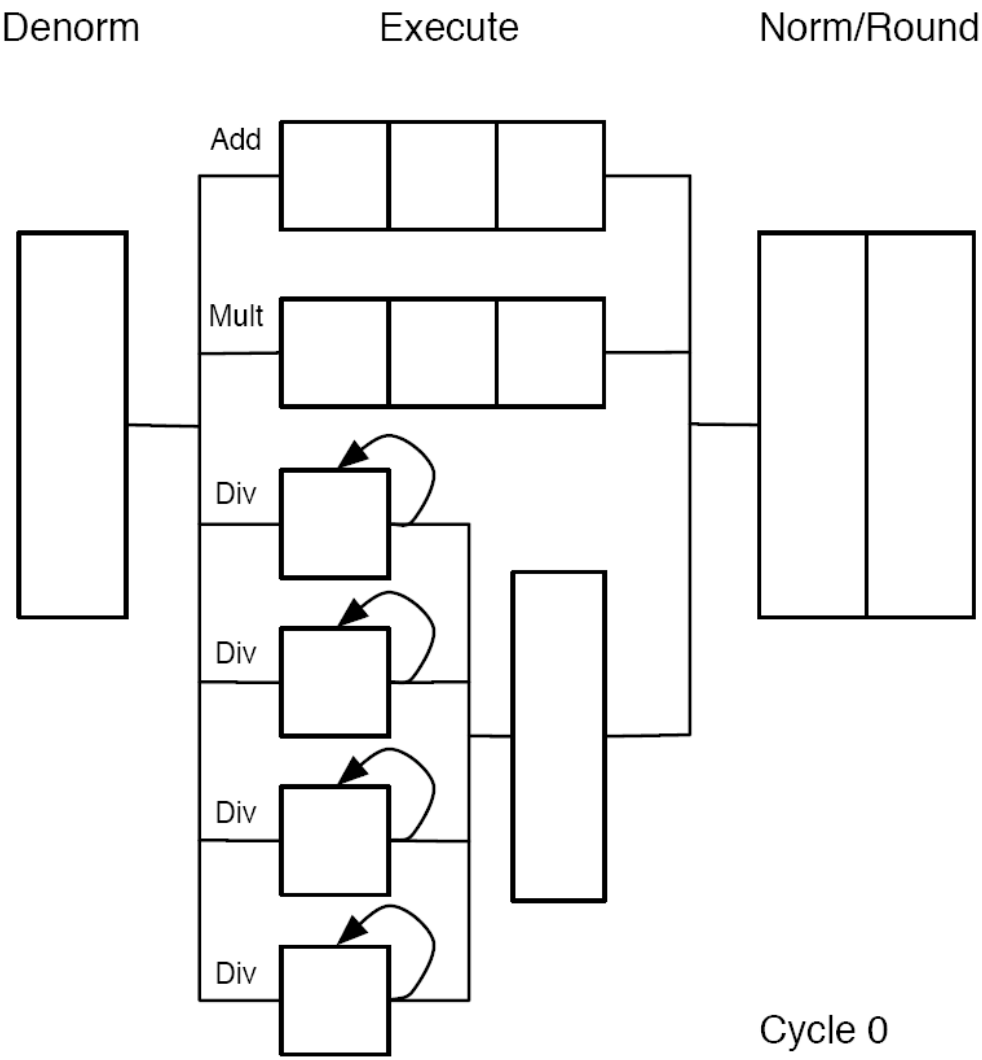
- IEEE-754 Compliant
  - SPARC V8 ISA Implementation
  - Single & Double Precision Floating Point
  - Fixed Point Arithmetic (Multiplication/Division)

- Worst Case FP Number of Cycles/Operation
  - Addition/Subtraction/Comparison = 6 Cycles
  - Multiplication = 6 Cycles
  - Division = 64 Cycles

- Short Term Goals
  - LEON3 SPARC V8 Compatibility
  - Square Root Implementation

Floating Point Unit

Floating Point Unit



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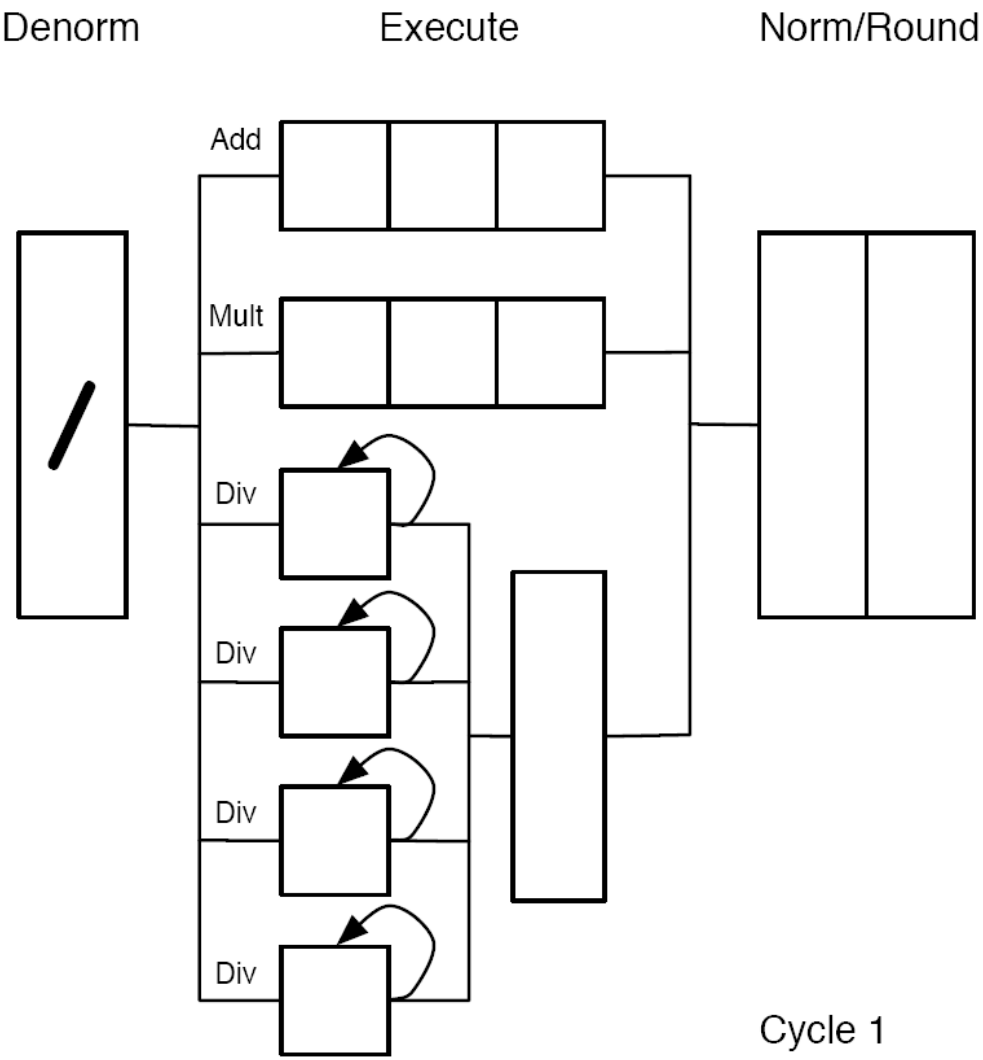

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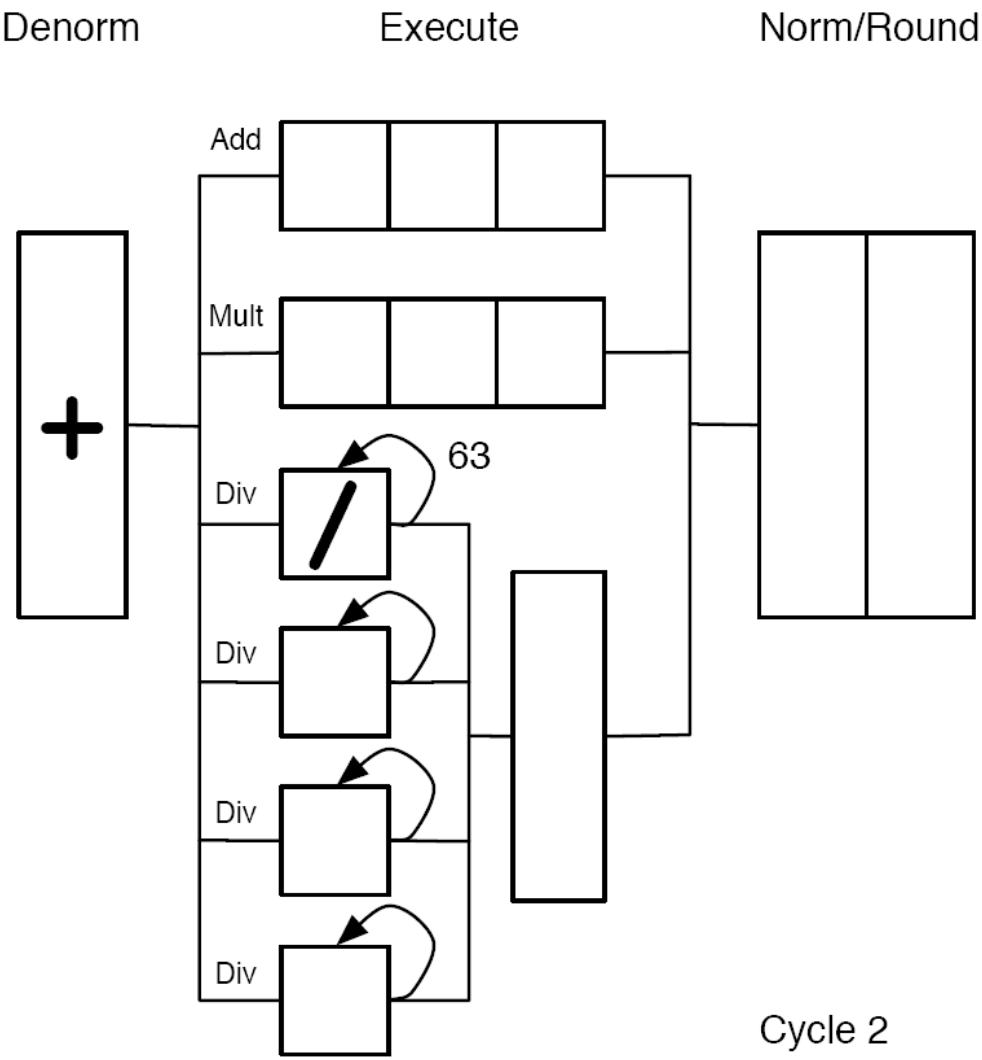

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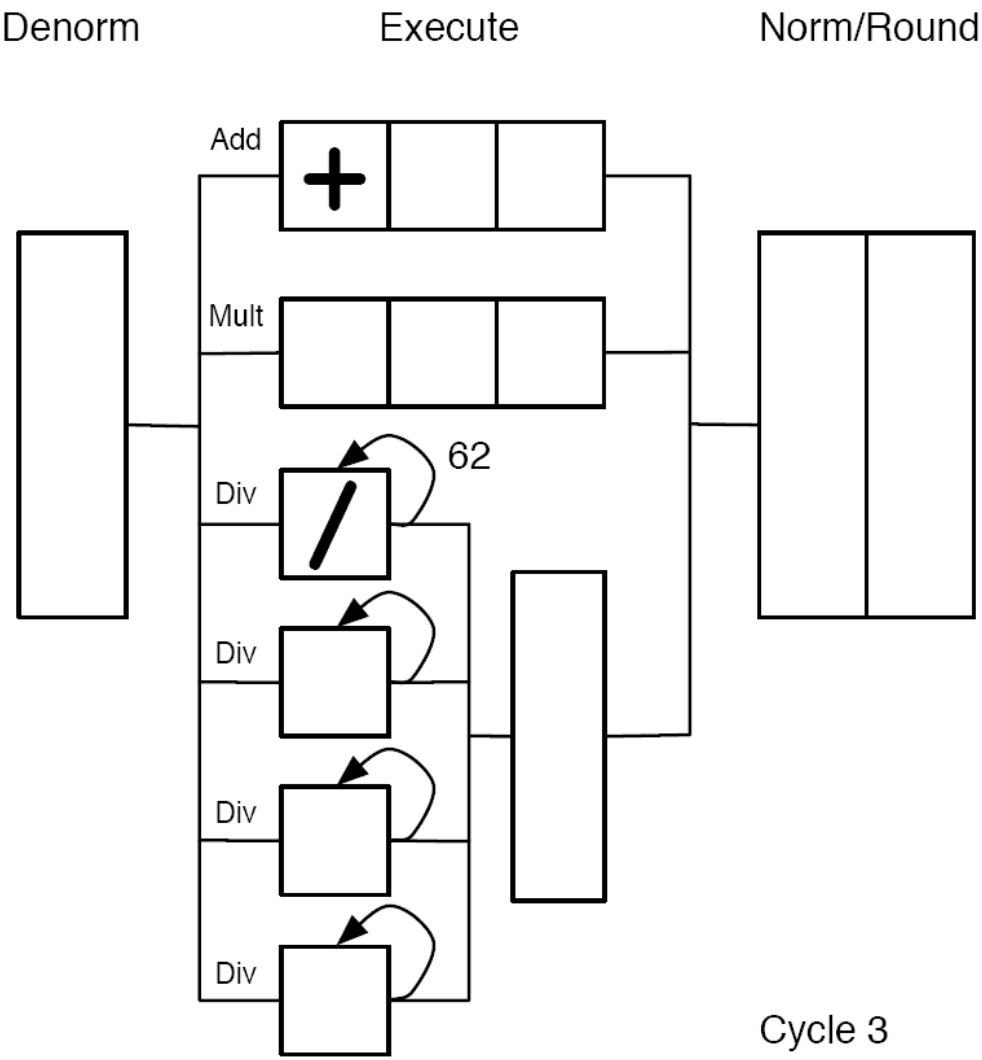

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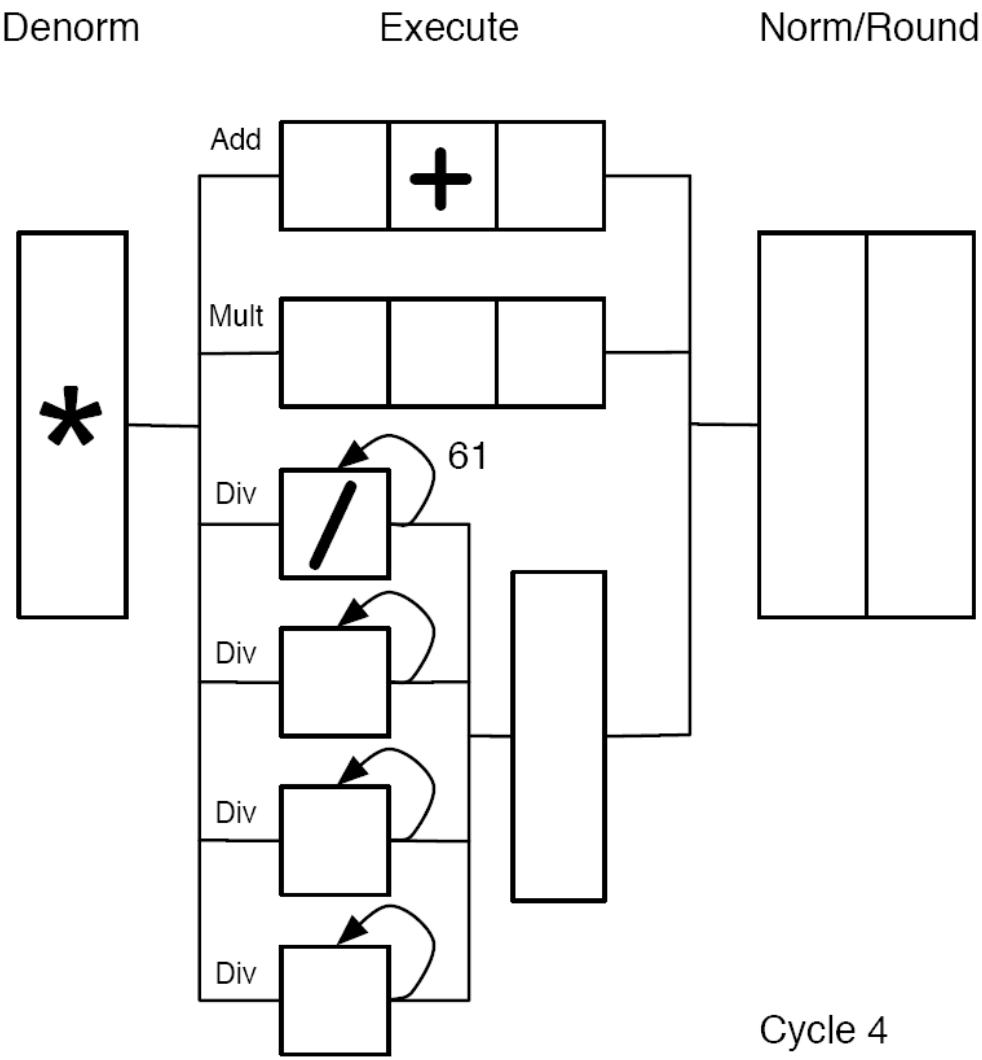

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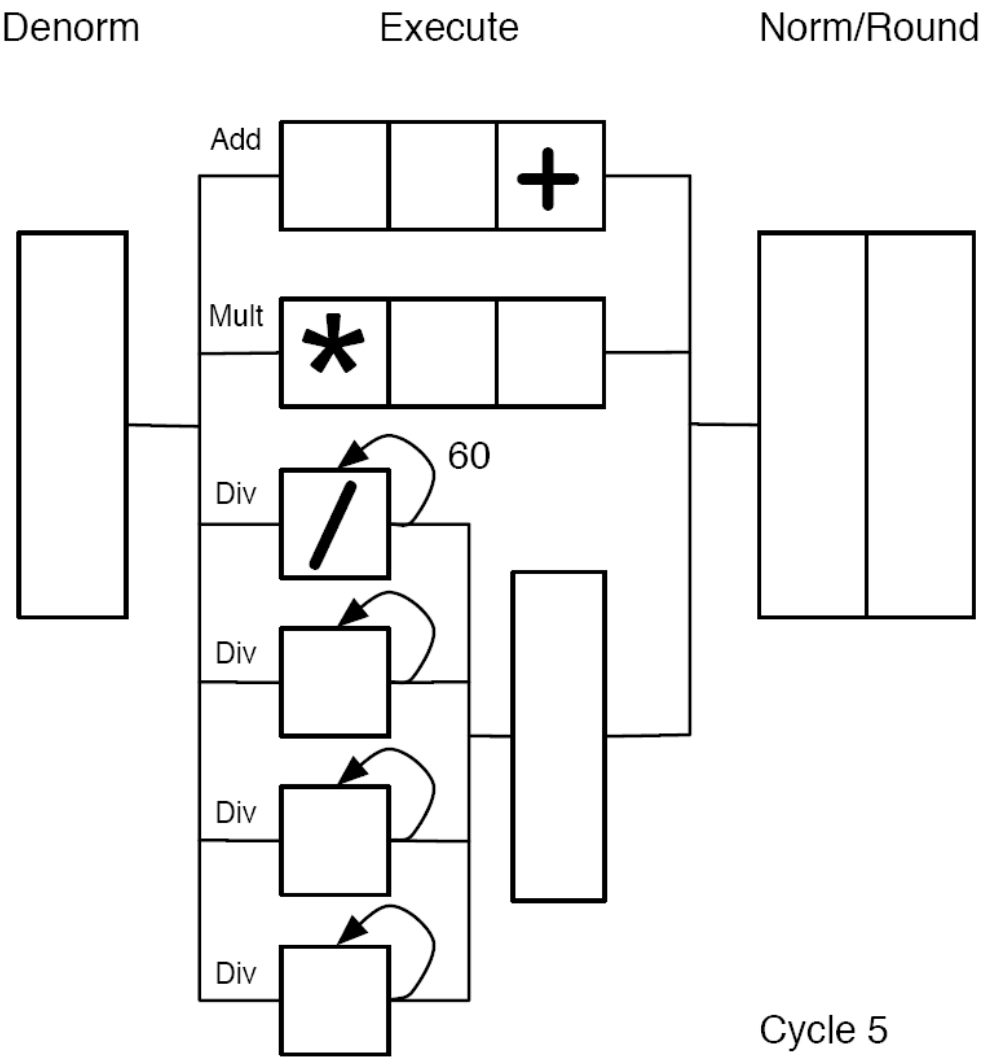

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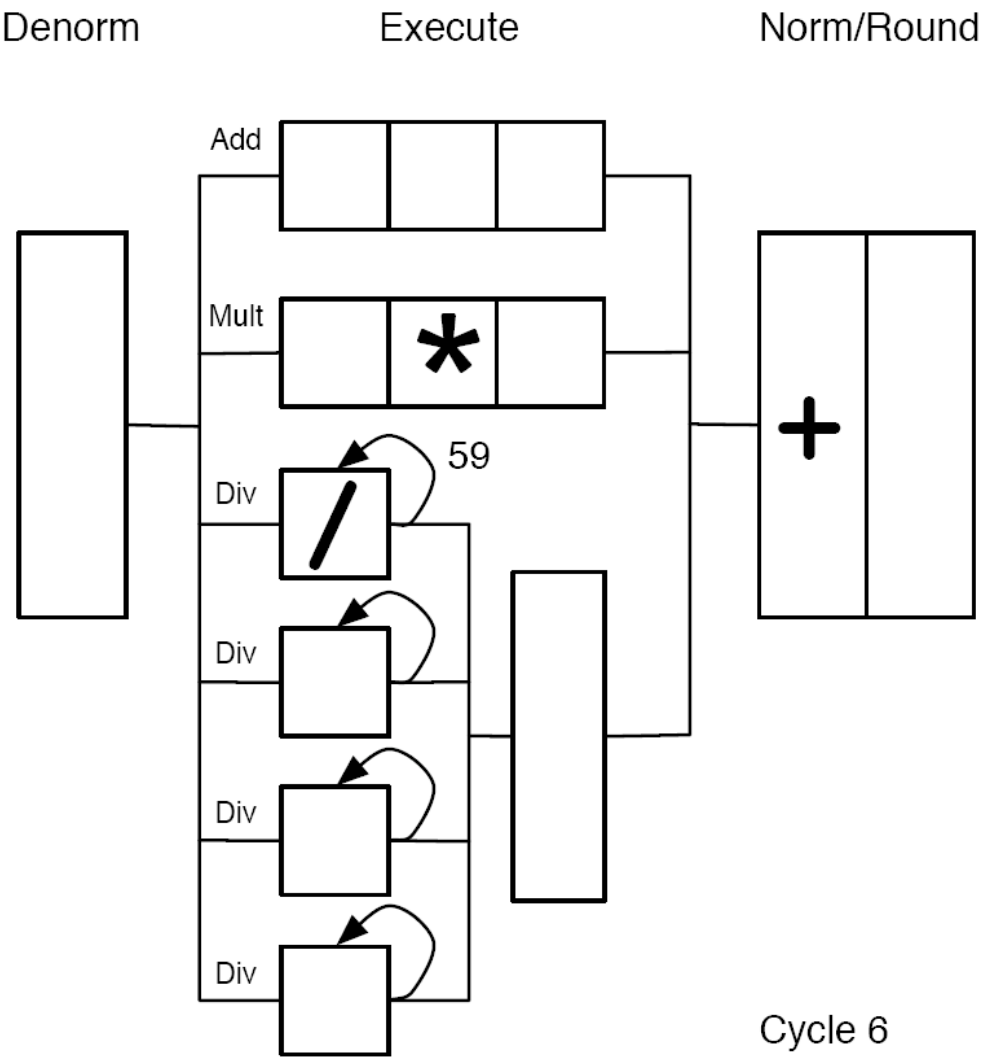

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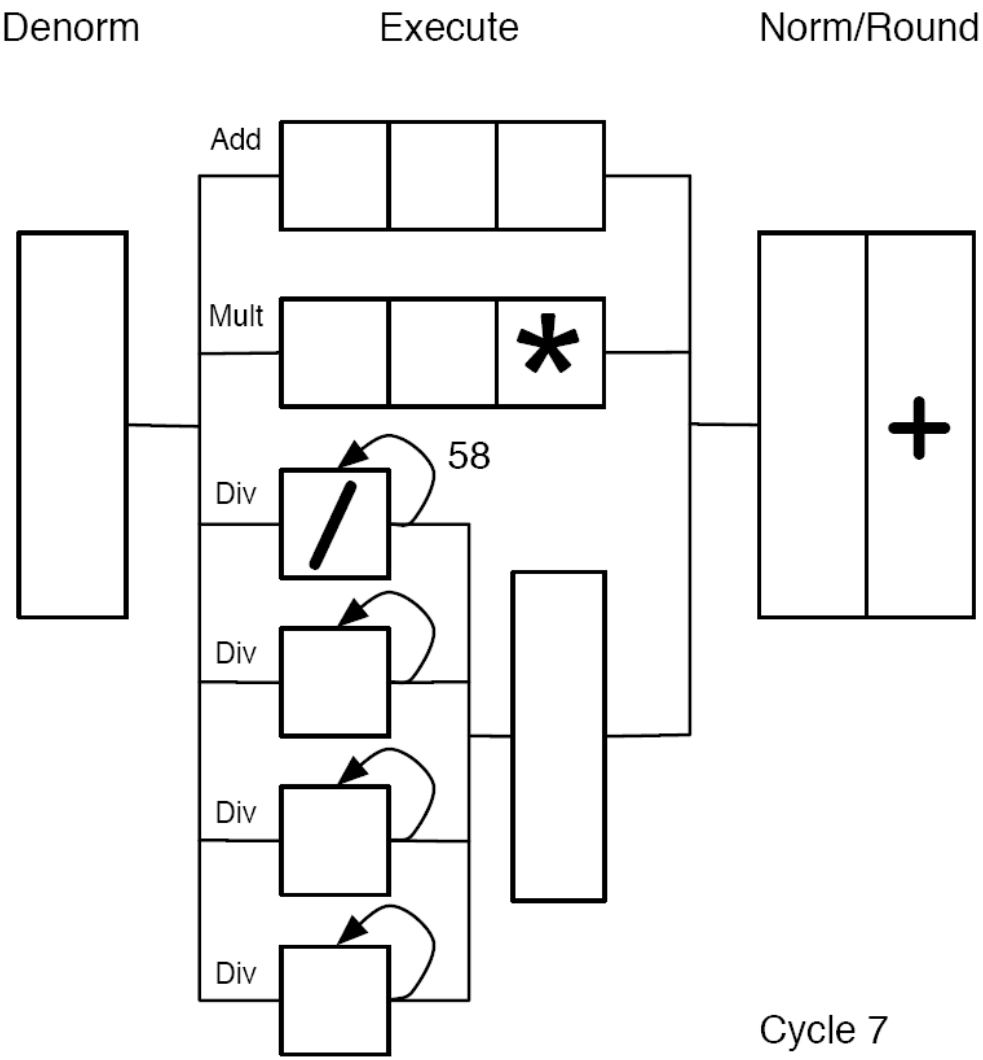

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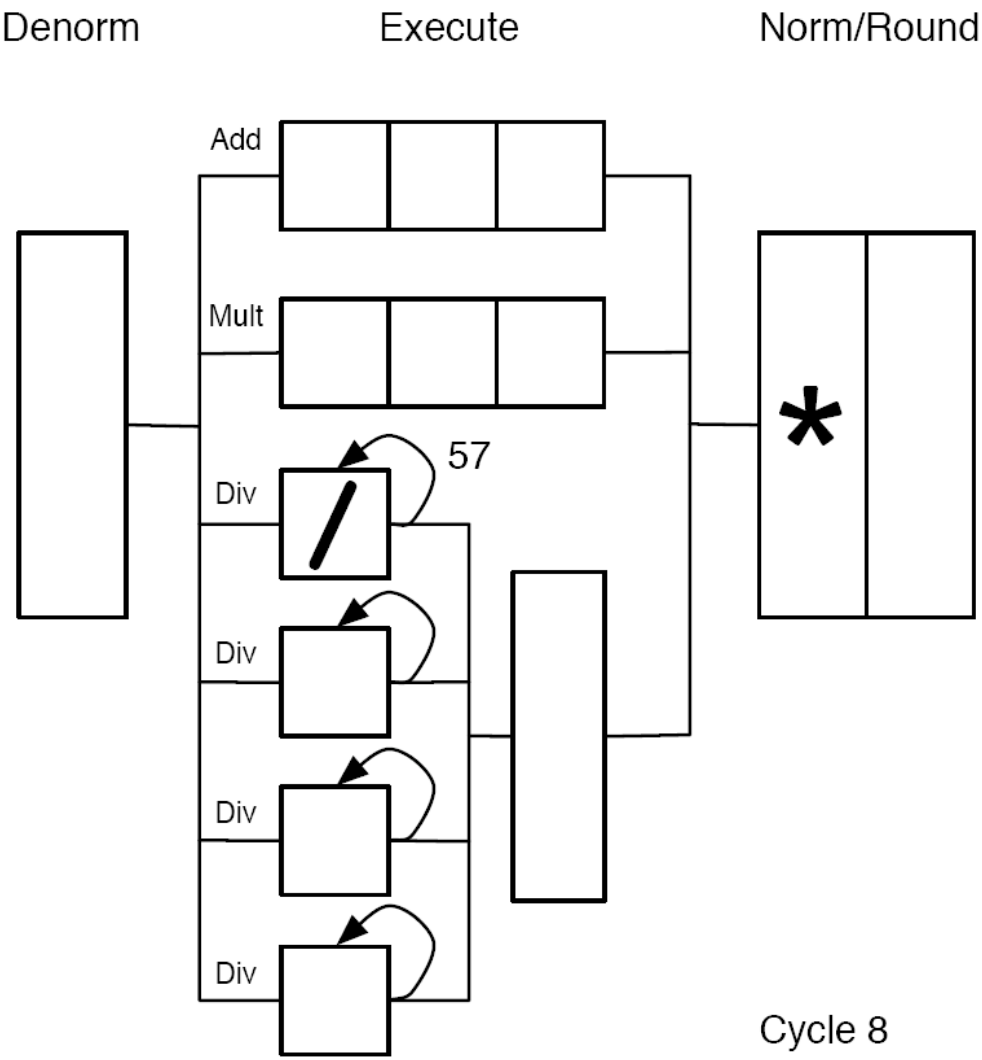

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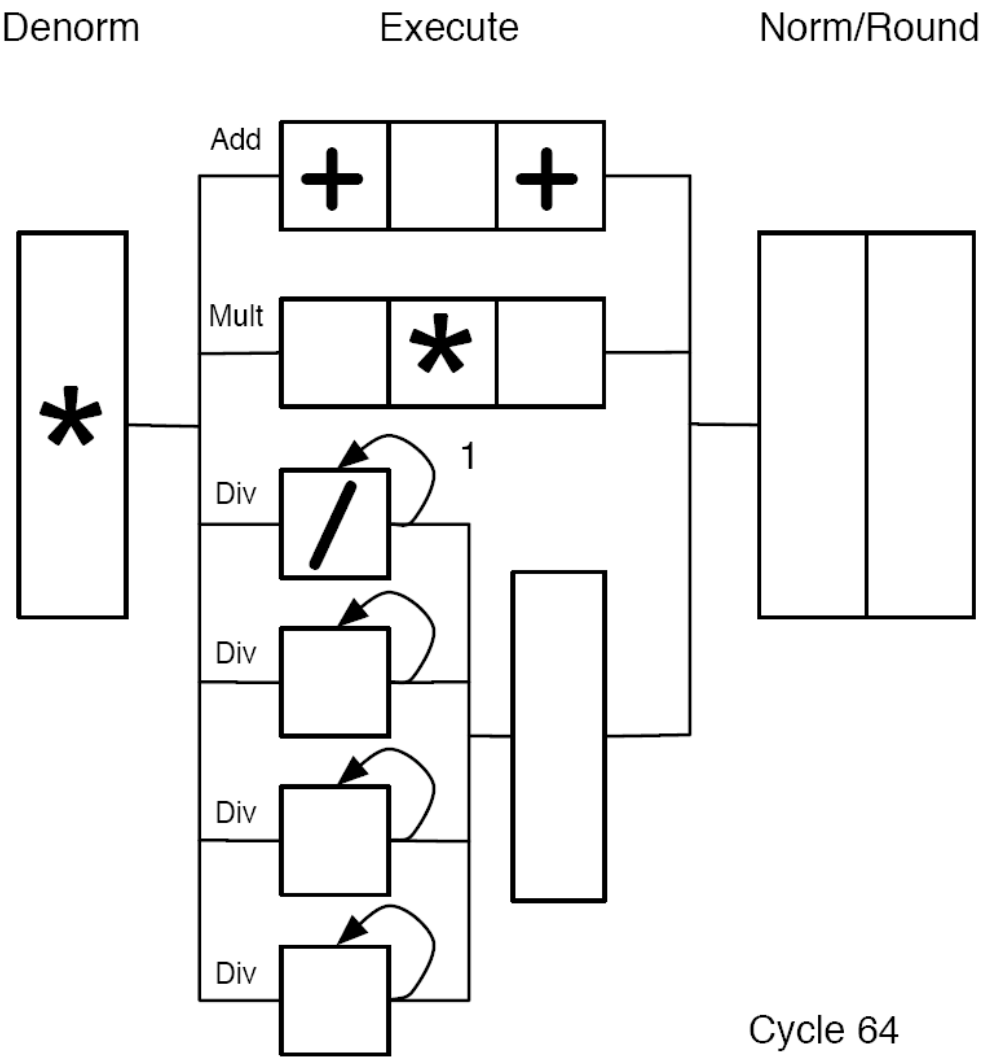

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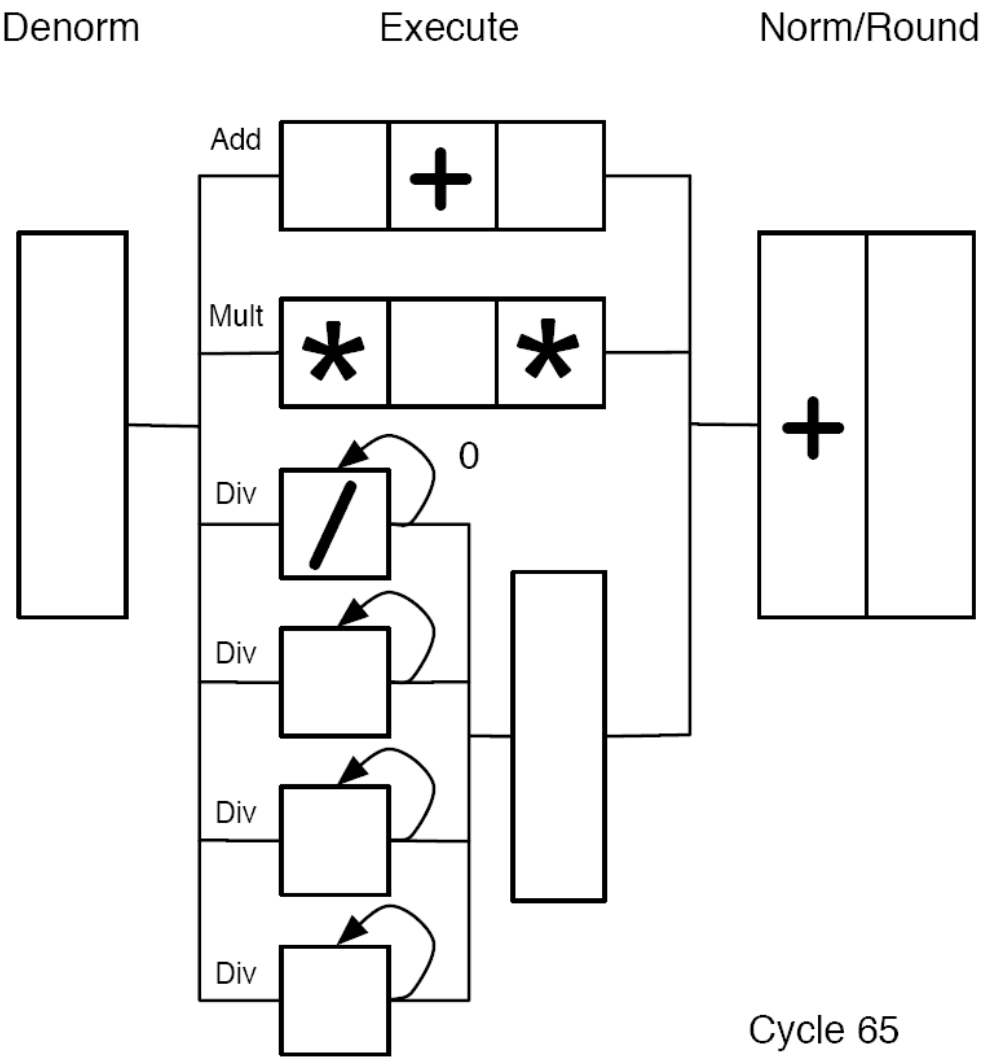

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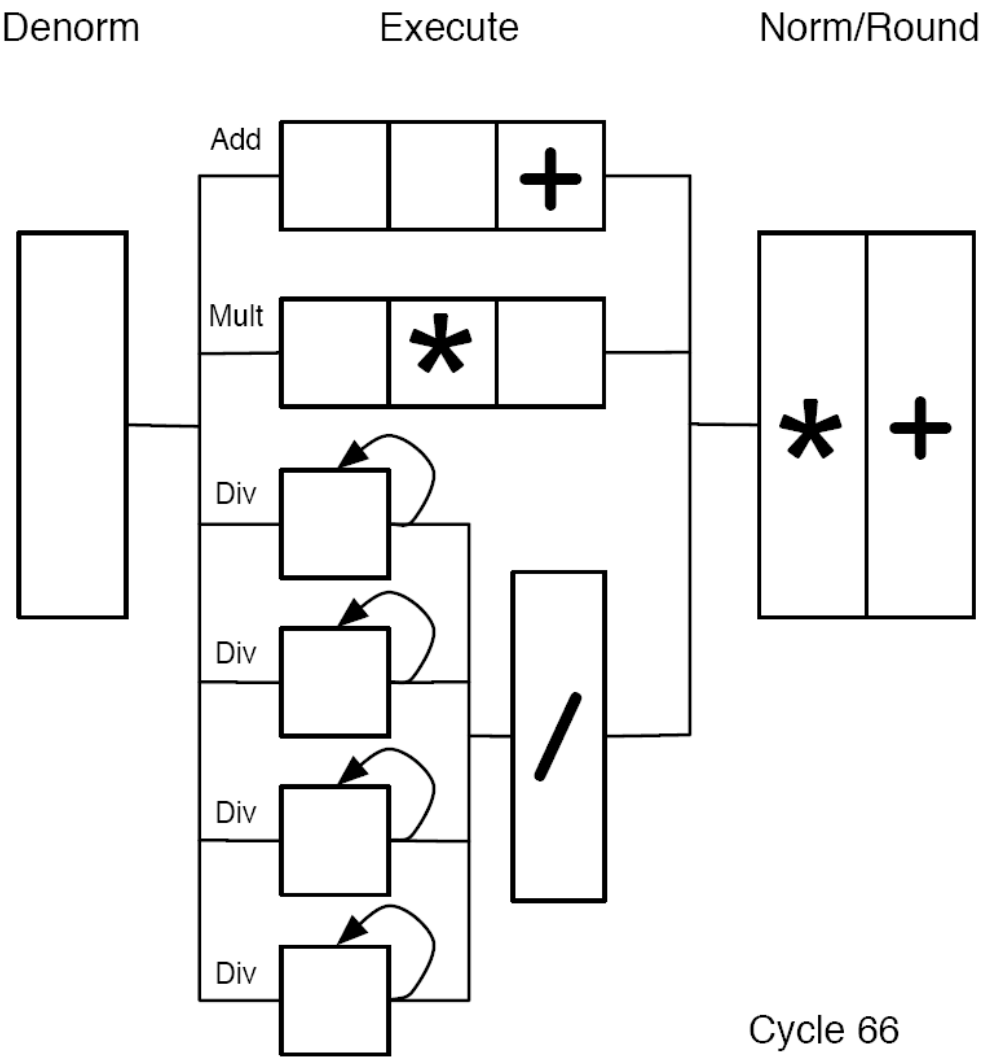

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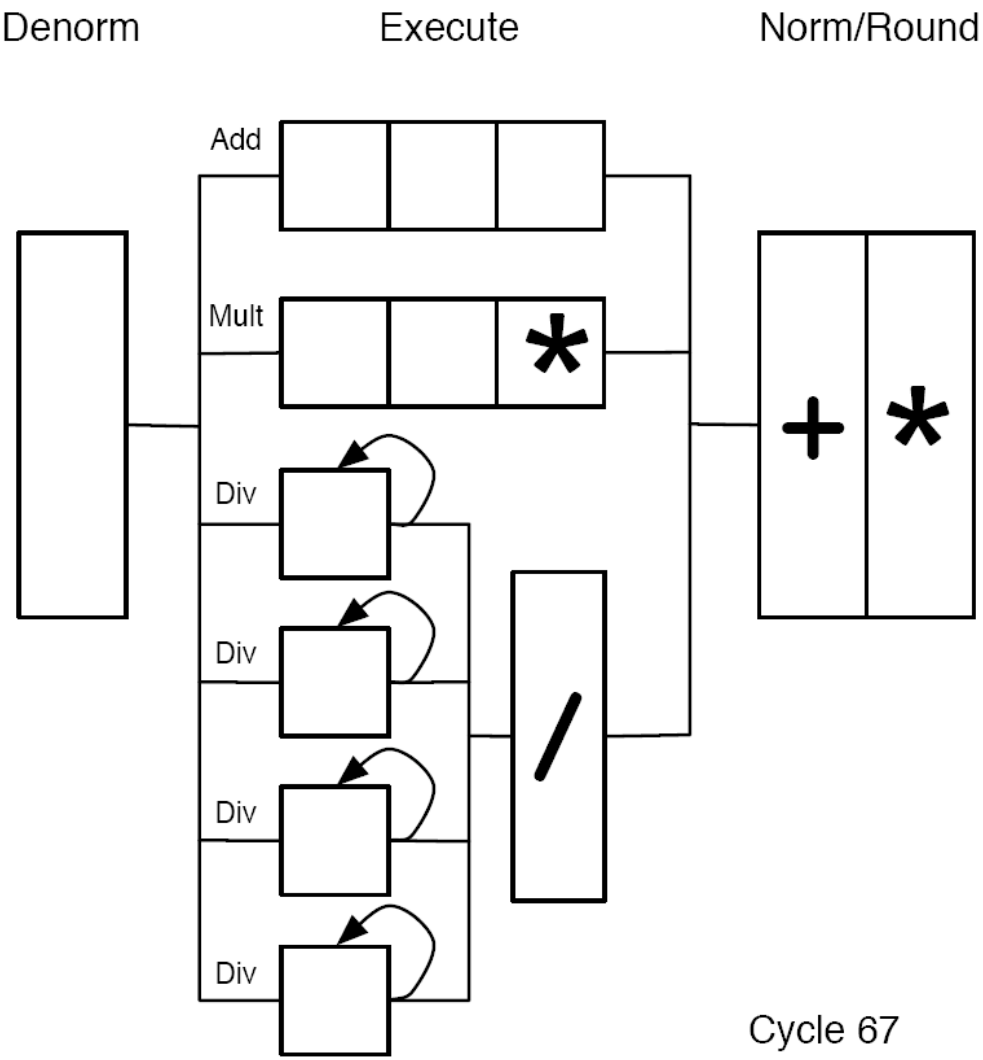

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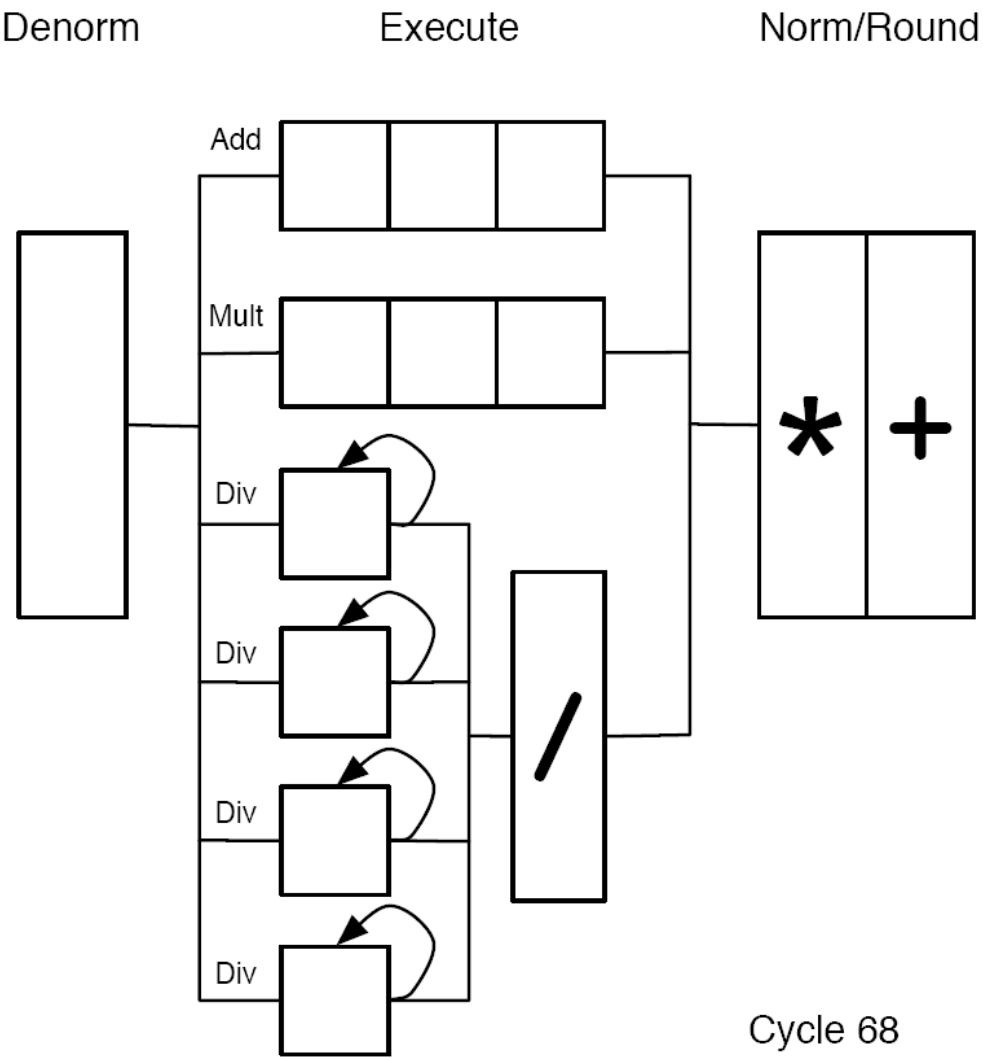

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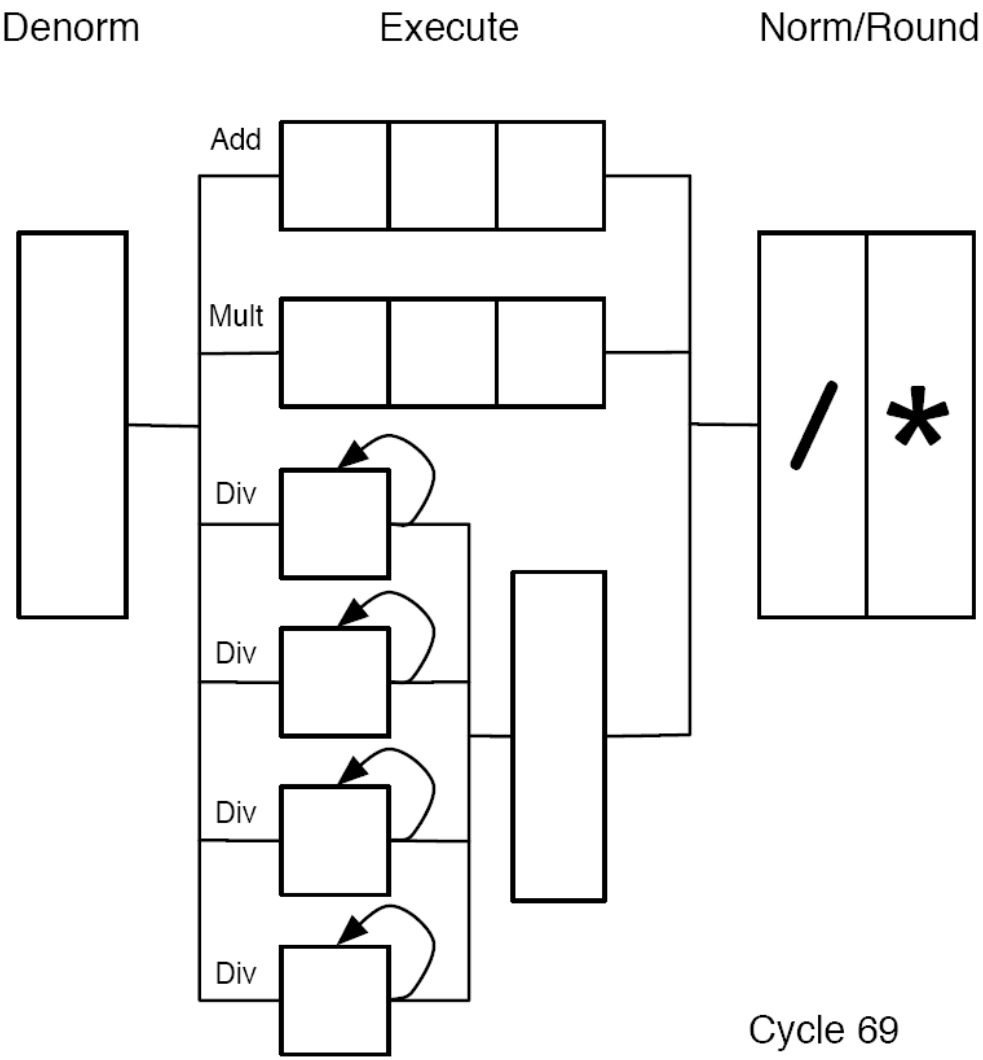
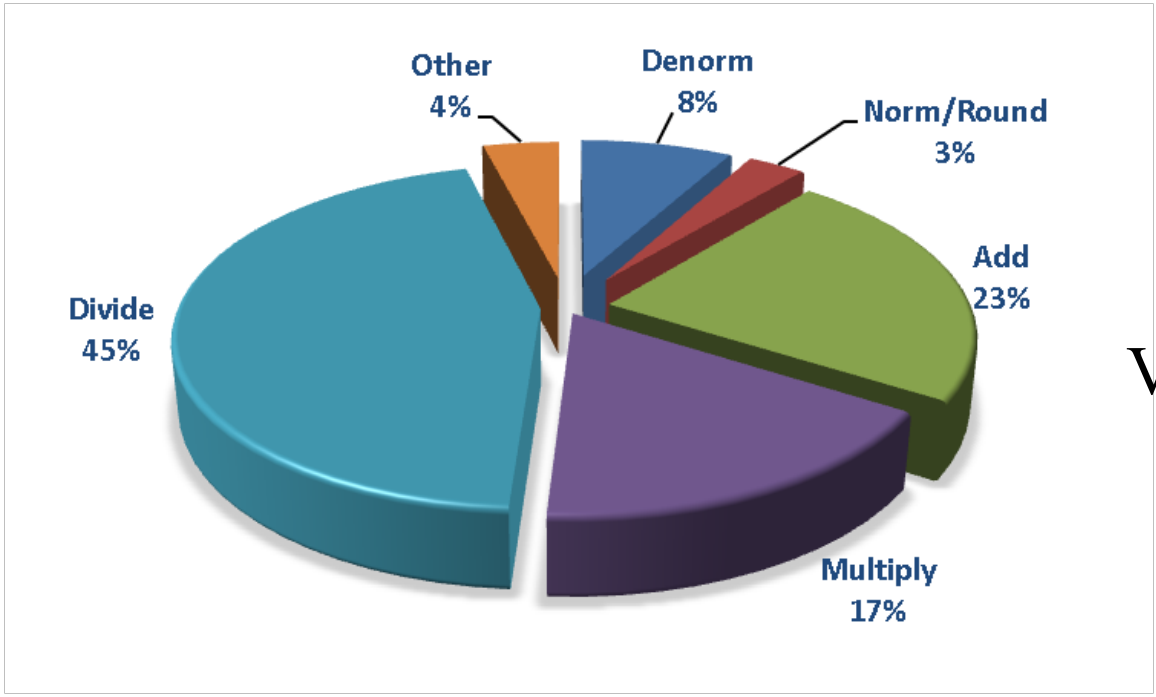


Simultaneous Synthesis Goals

- Dual FPGA & ASIC Synthesis
  - FPGA Prototype Implementation
  - ASIC is Ultimate Objective
- Major Optimization Goals
  - FPGA
    - Minimize LUT Utilization
  - ASIC
    - Achieve 1.4 GHz
    - Optimize Power

FPGA Synthesis Results

- ~6500 LUTs at 156 MHz (Xilinx Virtex-5)
- ~4000 ALMs at 143 MHz (Altera STRATIX II)



Virtex-5

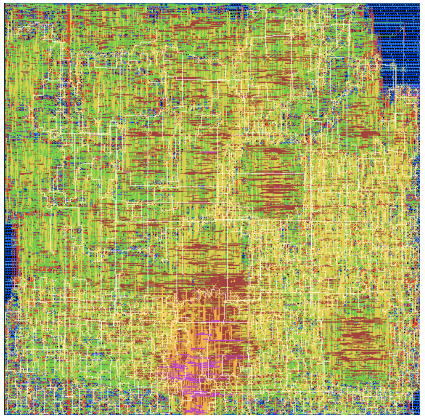
Comparison on Virtex-II

- Virtex-II
  - 130 nm Technology
- ~8900 LUTS at 97 MHz (SCOORE FPU)
- ~8500 LUTS at 65 MHz (LEON FPU)

ASIC

- Results For 90nm Technology:

	Front-End	Back-End
	DC_Shell	SoC Encounter
Frequency	1.3 GHz	1.4 GHz
Area	0.36mm^2	0.25mm^2
Power	67mW	--

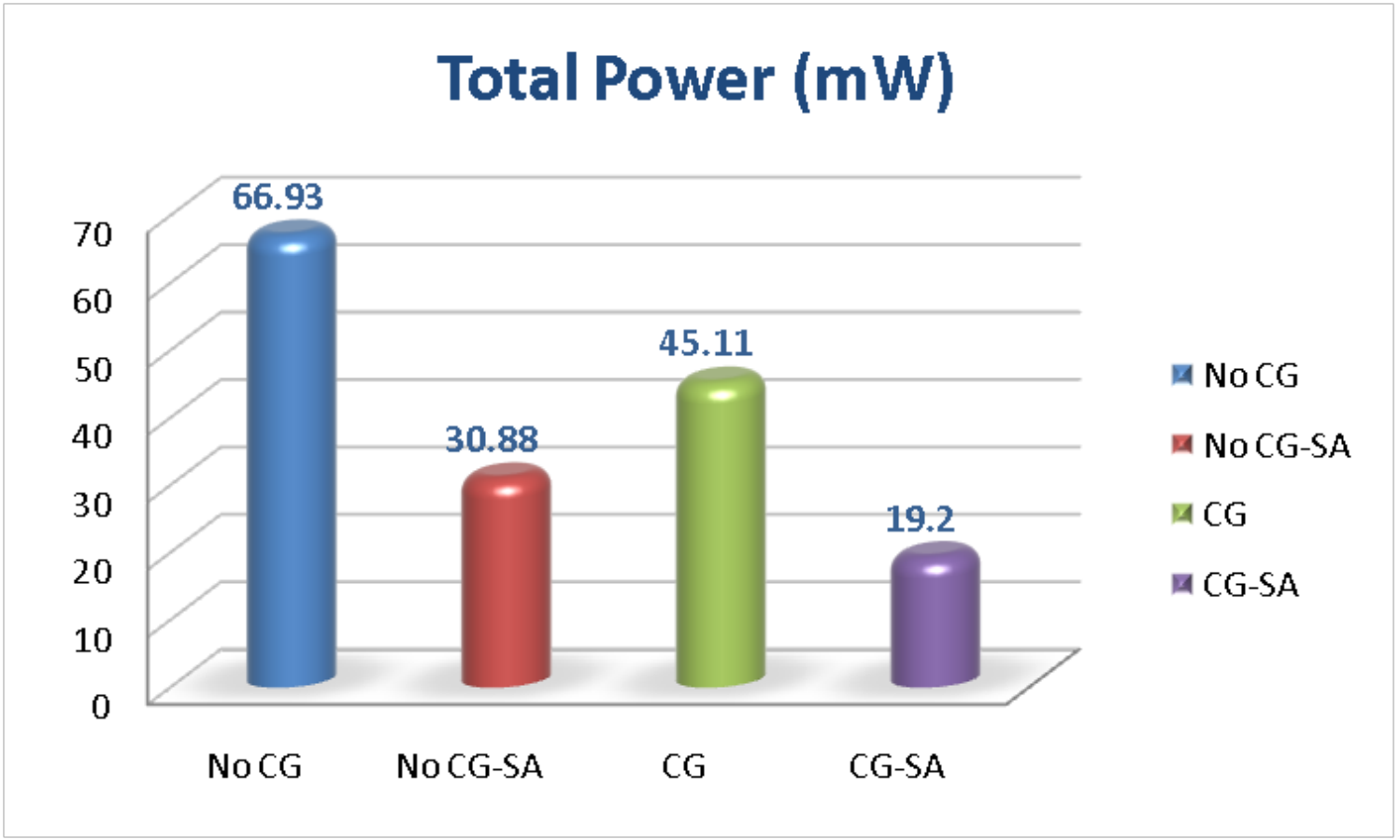


Physical View of FPU

ASIC Power Analysis

- FPU Natural Target for Power Savings
  - Frequent In-Activity
- Clock Gating
- Switching Activity
  - Total Number of Transitions Occurring at Every Gate Per a Given Benchmark

Clock-Gating Results



- ~30% Improvement in Power Consumption

Conclusion

- Open Source BSD License
- Complete Front to Back End Implementation
- Competitive ASIC Frequency
- Reasonable LUT Utilization
- Reasonable Power Optimization
- Comparable Alternative to Leon's FPU

Acknowledgments

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Thank You!

Rigo Dicochea

Website: http://masc.soe.ucsc.edu
Email: rigo@soe.ucsc.edu