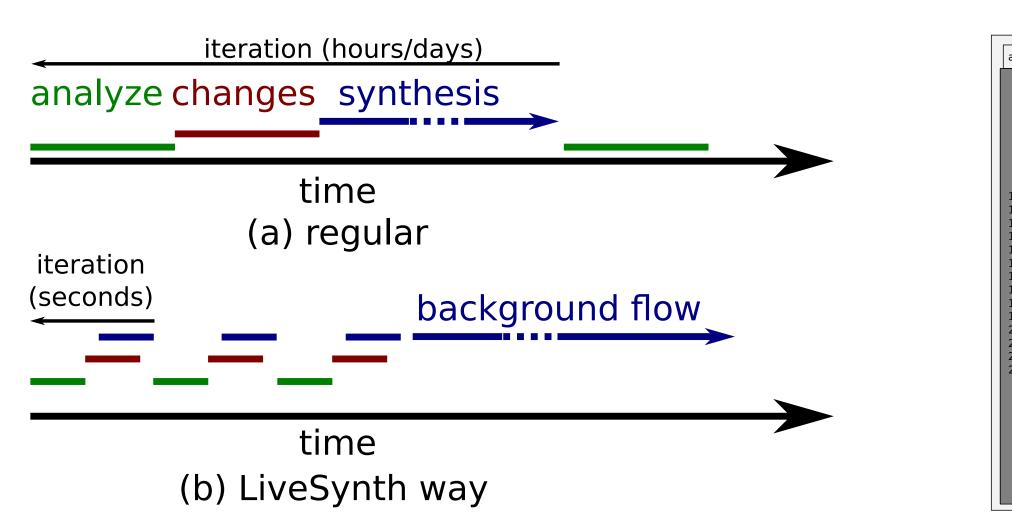


#### **Background:**

- $\rightarrow$  Synthesis is tedious and time consuming, especial
- $\rightarrow$  This contrasts with rapid development techniques
- $\rightarrow$  We expect designers productivity to improve with a

## Model:

- → LiveSynth targets interactive synthesis with feedb
- $\rightarrow$  LiveSynth allows designers to trigger synthesis mor
- $\rightarrow$  LiveSynth flow is divided into two phases:
  - → Interactive step: gives feedback in under a few
  - → Background step: high effort optimization, wh



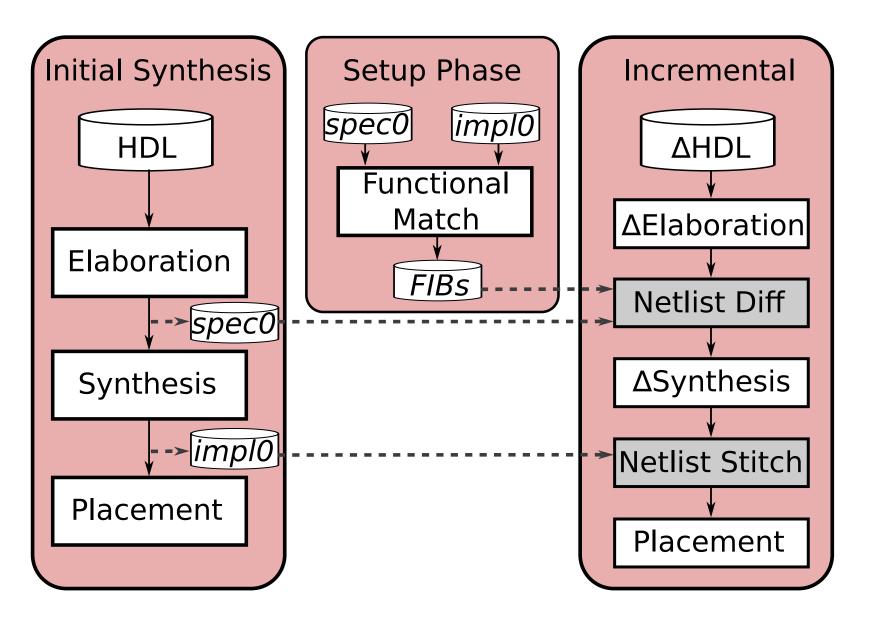
**Fig 1.** LiveSynth shifts the digital design paradigm to incremental changes, allowing for more interations per day.

#### **Incremental Flow:**

 $\rightarrow$  LiveSynth automatically defines regions of a few the  $\rightarrow$  Invariant cones [1] are regions whose functionality LiveSynth.

 $\rightarrow$  During the incremental step, only cones that were

 $\rightarrow$  To avoid impact on QoR, if the critical path is hit, the



**Fig 3.** The initial synthesis is performed as usual, and the incremental step is performed when the designer changes the RTL.

# LiveSynth: Towards an Interactive Synthesis Flow

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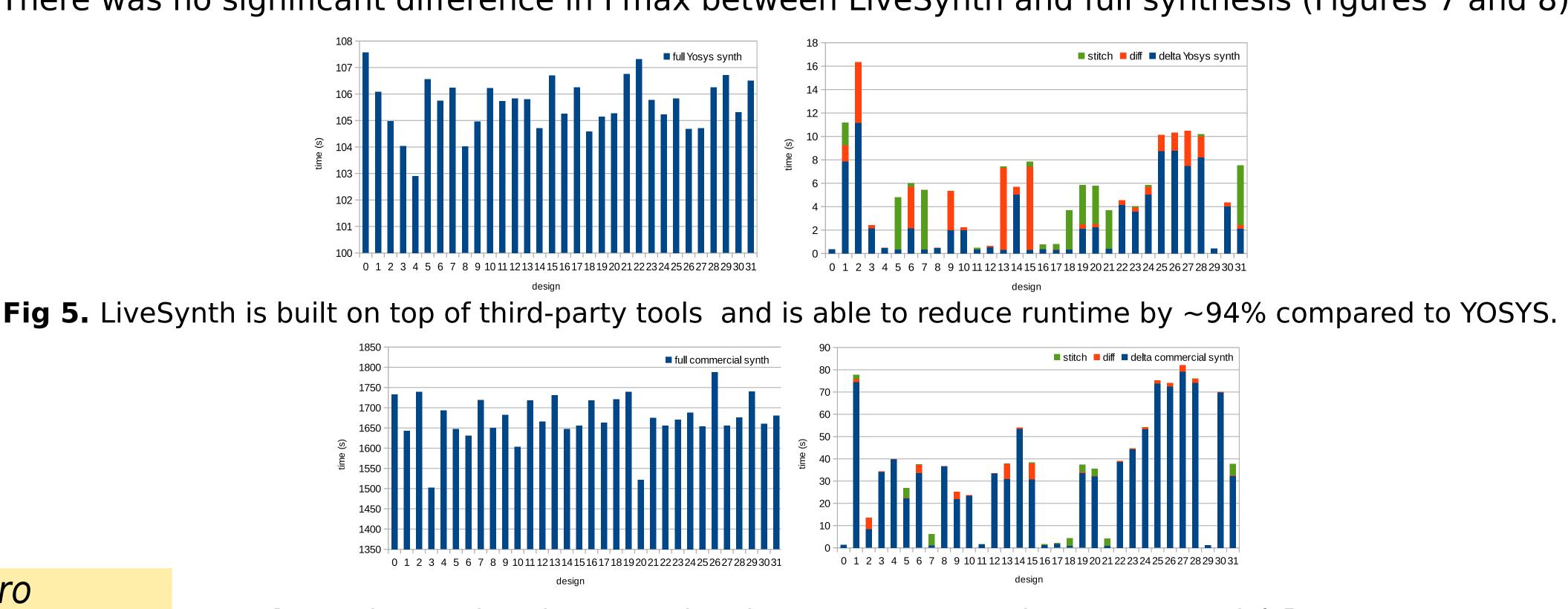
ly during the timing/power closure cycle. popular in software engineering. an interactive synthesis environment.		Set → V → V → 3 → L
back within a few ore frequently and w seconds, with h hen the designer is	incrementally.	<b>Re</b> : → 7 → 7
<pre>input clk; input reset; input [size-1:0] d; output [size-1:0] q; output [size-1:0] qb; reg q; assign qb = ~q; alway @(posedge clk or posedge reset) begin if(reset) begin //async reset q &lt;= 1'b0; end else begin q &lt;= d; end end endmodule</pre>	Project info: Messages:   Project name: FPU Errors: 0   Top module: fpu.v Warnings: 2   Target: 32nm Information: 5   Worst negative slack: -0.1 ns Power information:   Worst negative slack: -0.5 ns Newmber of failing endpoints: 5   Neumber of failing endpoints: 5 Switch Leakage Total   Clock 0.50 0.00   Setup Hold	
As the design new resul		Micr Arc Sa
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A A B A B A A A A A A A A A A A A A A A	ementation ementation e boundaries are present over esigns and provide for incremental synthesis.	Fu $\rightarrow$   $\rightarrow$   $\rightarrow$   $\rightarrow$ F Ac This CNS exp Refe
		[1] D

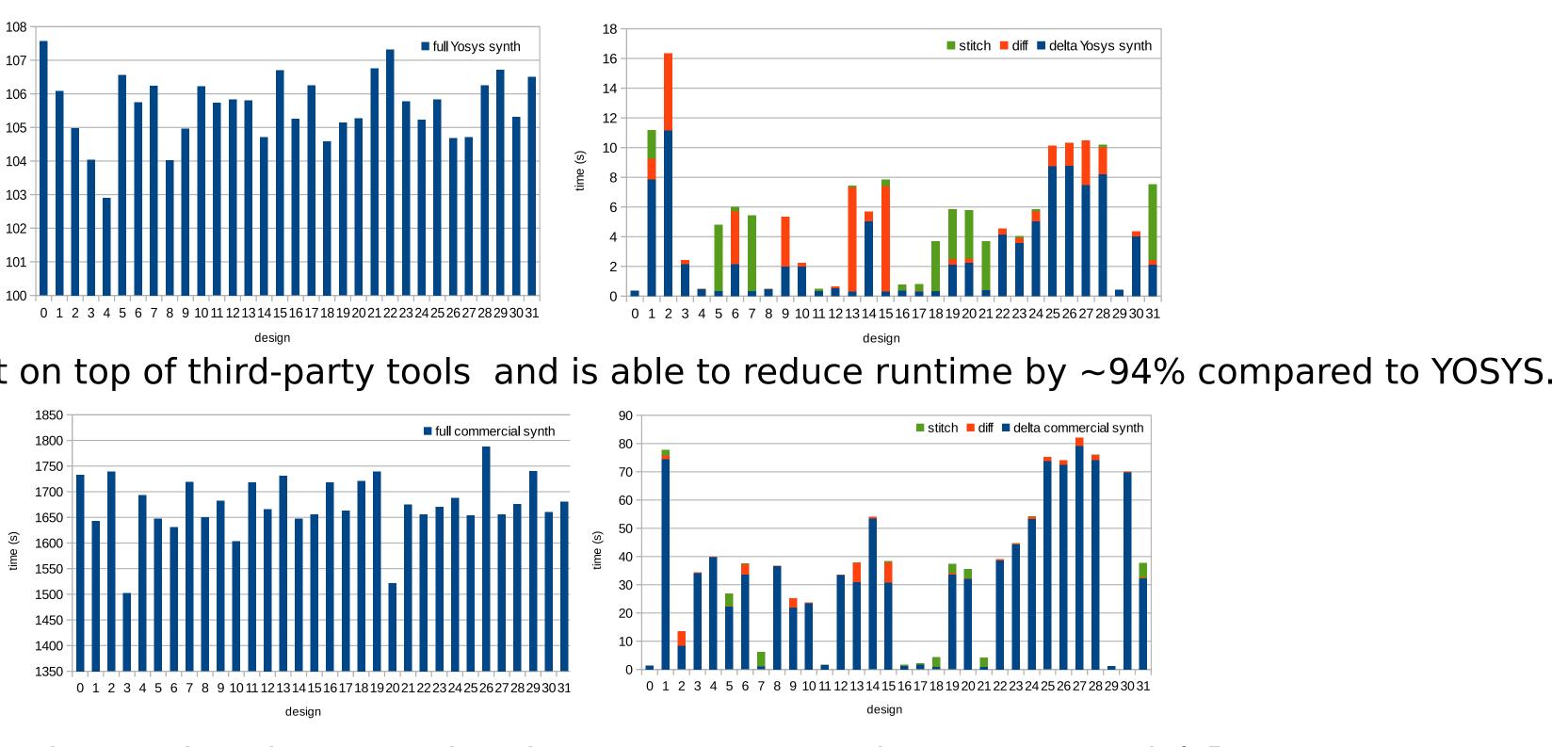
### tup:

We implemented the incremental step of LiveSynth in Ruby. We used an in-house FPU verilog code as benchmark. 32 changes were added in randomly choosen locations, activated through define statements. \_iveSynth was run on-top of a commercial flow and YOSYS [2], an open-source synthesis tool.

#### sults:

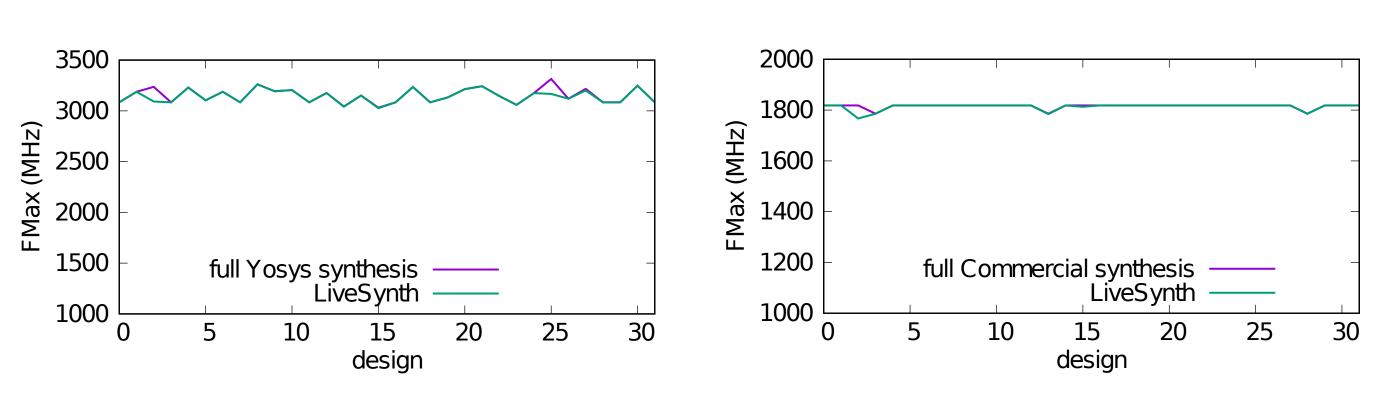
The incremental step of LiveSynth achieves  $\sim$ 95% faster synthesis than a full run (Figures 5 and 6). There was no significant difference in Fmax between LiveSynth and full synthesis (Figures 7 and 8).





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**Fig 6.** LiveSynth reduces runtime by  $\sim$ 96% compared to a commercial flow.



**Fig 7.** LiveSynth is able to deliver the same QoR as the full synthesis, with minor fluctuations.

#### onclusion:

The incremental step of LiveSynth reduces synthesis time by about 95% for incremental changes. LiveSynth shifts the paradigm to small, incremental changes and more iterations per day. We advocate for an interactive synthesis flow as a way to boost design productivity.

#### iture Work:

Incremental back-end to further improve on feedback accuracy. Improve synthesis to reduce QoR impact.

Further reduce synthesis area to reduce synthesis time in the outliers. FPGA target with further improvement on backend.

#### knowledgments:

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#### erences:

D. Chen and D. Singh, "Line-level incremental resynthesis techniques for fpgas," in FPGA'11. [2] C. Wolf. Yosys open synthesis suite. http://www.clifford.at/yosys/



