Validation
ESESC Tutorial

Speaker: Ethan Papp

ESESC

Department of Computer Engineering,
University of California, Santa Cruz
http://masc.soe.ucsc.edu

UC SANTA CRUZ

Validation

- You will learn:
  - Validation of ESESC with an ARM A15 (Samsung Chromebook)
  - Single and multi process validation of:
    - IPC
    - IL1 cache miss rate
    - DL1 cache miss rate
    - LLC cache miss rate
    - Branch Predictor miss rate
    - Global cache miss rate
    - TLB miss rate

Validation Overview

- Validate ESESC against Samsung Chromebook via SPEC CPU benchmarks
- Used Perf utility on Chromebook with performance counters enabled
- Modeled ARM a15 in ESESC simu.conf file
- Run for 3 billion instructions

ESESC ARM A15 Cache Parameters

```
[IL1_core]
deviceType          = 'icache'
blockName           = "Icache"
coreCoupledFreq     = true
inclusive           = true
directory           = false
numBanks            = 1
maxRequests         = 32
size                = 32*1024
assoc               = 2
bsize               = 64
replPolicy          = 'LRU'
bkNumPorts          = 1
bkPortOccp          = 1
hitDelay            = 2
missDelay           = 2
MSHR                = "IL1MSHR"
lowerLevel          = "PrivL2 L2 shared"
pfetchBuffSize    = 16

[IL1MSHR]
size                = 4
type                = "full"
nSubEntries         = 8

[PerCore_DTLB]
deviceType          = 'tlb'
blockName           = "PTLB"
numPorts            = 0
hitDelay            = 0
size                = 32 * 4096
assoc               = 32
bsize               = 4*1024
replPolicy          = 'LRU'
lowerLevel          = "DL1_core DL1"
lowerTLB            = "Shared_TLB STLB shared"
lowerTLB_delay      = 12 # 20
```

- Icache size
- Cache delays
- Cache hierarchy

ESESC ARM A15 Cache Parameters cont.

```
[PerCore_ITLB]
deviceType          = 'tlb'
blockName           = "PTLB"
numPorts            = 0
hitDelay            = 0 # delay charged in L1
size                = 32 * 4096 # 64*4096
assoc               = 32 #  64
bsize               = 4*1024
replPolicy          = 'LRU'
lowerLevel          = "IL1_core IL1"
lowerTLB            = "Shared_TLB STLB shared"
lowerTLB_delay      = 20

[DL1_core]
deviceType          = 'cache'
coreCoupledFreq     = true
inclusive           = true
directory           = false
blockName           = "dcache"
size                = 32*1024
assoc               = 2
skew                = false
bsize               = 64
replPolicy          = 'LRU'
hitDelay            = 3 #+1 from the ALU
missDelay           = 1
MSHR                = "DL1_MSHR"
lowerLevel          = "PrivL2 L2 shared"   # I
fillBuffSize        = 4
pfetchBuffSize      = 16
wbBuffSize          = 16
port                = "DL1_corePort"
```

- TLB options
- dCache options

ESESC ARM A15 Cache Parameters cont.

```
[tradCORE]
scooreCore          = false
areaFactor          = 2
fetchWidth          = 4
fetchPorts          = 1
instQueueSize       = 4
inorder             = false
throttlingRatio     = 1.0
issueWidth          = 8 #chromebook
retireWidth         = 3 #chromebook
decodeDelay         = 3 #chromebook
renameDelay         = 2 #chromebook
maxBranches         = 1024
bb4Cycle            = 1
bpredDelay          = 2
maxIRequests        = 2
interClusterLat     = 1 #chromebook
clusterScheduler    = "RoundRobin"
cluster[0]          = 'AUNIT'
cluster[1]          = 'BUNIT'
cluster[2]          = 'CUNIT'
#cluster[3]         = 'LUNIT' #'MUNIT' #chromebook 'LUNIT'
cluster[3]          = 'LSUNIT' #'LSUNIT' #chromebook 'SUNIT'
bpred               = 'BPredIssueX2' #chromebook 'BPredIssueX'
robSize             = 128 # chromebook
stForwardDelay      = 3  # +1 clk from the instruction latency
maxLoads            = 128 #chromebook
maxStores           = 128 #chromebook
DL1                 = "PerCore_DTLB PTLB"
IL1                 = "PerCore_ITLB ITLB"
NoMemoryReplay      = true #chromebook
enableICache        = true
enableDCache        = true
noMemSpec           = true #chromebook
StoreSetSize        = 8192
instWidth           = 32
opcodeWidth         = 11
nArchRegs           = 32
```

- Core parameters
- OoO parameters
- ~/projs/esesc/conf/simu.conf.exynos4

Parameters Modeled

We can “properly” model in ESESC:

- Cache hierarchy
  - size
  - levels
  - associativity
- Memory bandwidth
- TLB
- Many OoO parameters

Chromebook validation setup

Sample Perf input

- perf stat -I 1941 -B -e instructions,cycles ./launcher -- stdin crafty.input – crafty
- perf stat -I 1941 -B -e L1-icache-loads,L1-icache-load-misses ./launcher -- stdin crafty.input – crafty
- perf stat -I 1941 -B -e L1-dcache-loads,L1-dcache-load-misses,L1-dcache-stores,L1-dcache-store-misses ./launcher -- stdin crafty.input – crafty
- perf stat -I 1941 -B -e LLC-loads,LLC-load-misses,LLC-stores,LLC-store-misses ./launcher -- stdin crafty.input – crafty

Chromebook validation setup

- Sample output

< 0.1 % runtime difference

< 1 % instruction count difference

```
             time             counts unit events
          .89916         3104168756      instructions
          .89916         3295342353      cycles

#             time             counts unit events
     1.941196125         1173543319      L1-icache-loa
     1.941196125           53403232      L1-icache-loa

#             time             counts unit events
     1.941204125          949002211      L1-dcache-loads
     1.941204125           37956823      L1-dcache-load-misses
     1.941204125          468808517      L1-dcache-stores
     1.941204125            3291618      L1-dcache-store-misses

#             time             counts unit events
     1.941196460          103790699      LLC-loads
     1.941196460             513730      LLC-load-misses
     1.941196460           51097459      LLC-stores
     1.941196460              55679      LLC-store-misses

#             time             counts unit events
     1.941190375          304378991      branches
     1.941190375           17982484      branch-misses

#             time             counts unit events
     1.941178293         3076550461      instructions
     1.941178293           57311027      dTLB-load-miss
     1.941178293            5843145      dTLB-store-miss
```

Individual Benchmarks

SPEC CPU 2000

- crafty
- gcc
- mcf
- mgrid
- wupwise
- swim
- applu
- equake
- mesa
- art
- vortex
- twolf

SPEC CPU 2006

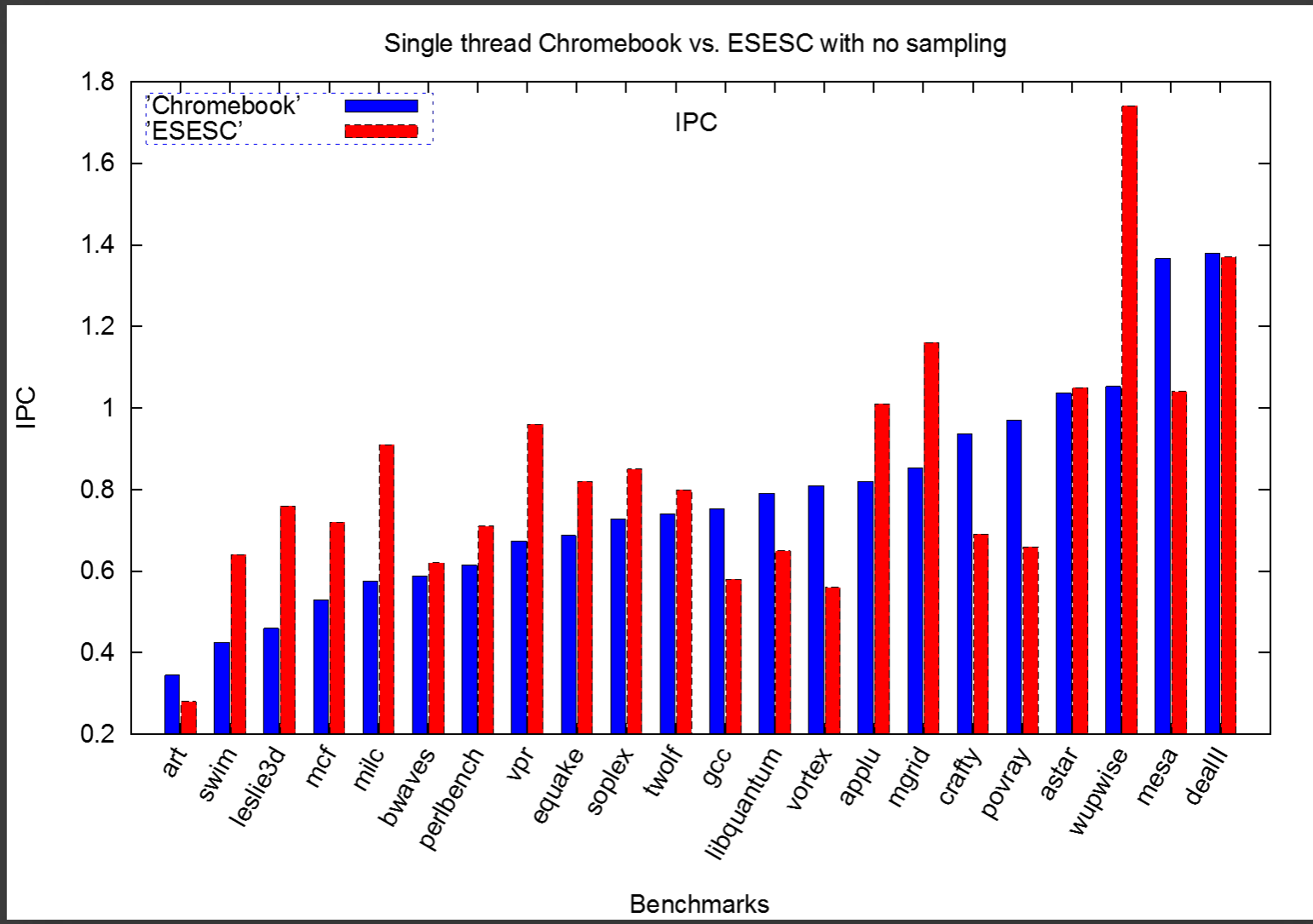
- leslie3D
- perlbench
- povray
- deal II
- bwaves
- vpr
- soplex
- milc
- libquantum
- astar

SPEC Rate-like Benchmarks

- mcf, mcf
- mesa, equake
- gcc, twolf
- applu, povray
- crafty, namd
- mcf, swim

- vpr, bwaves
- libquantum, milc
- deal II, perlbench
- mesa, wupwise
- vortex, leslie3D
- mgrid, astar

IPC Results

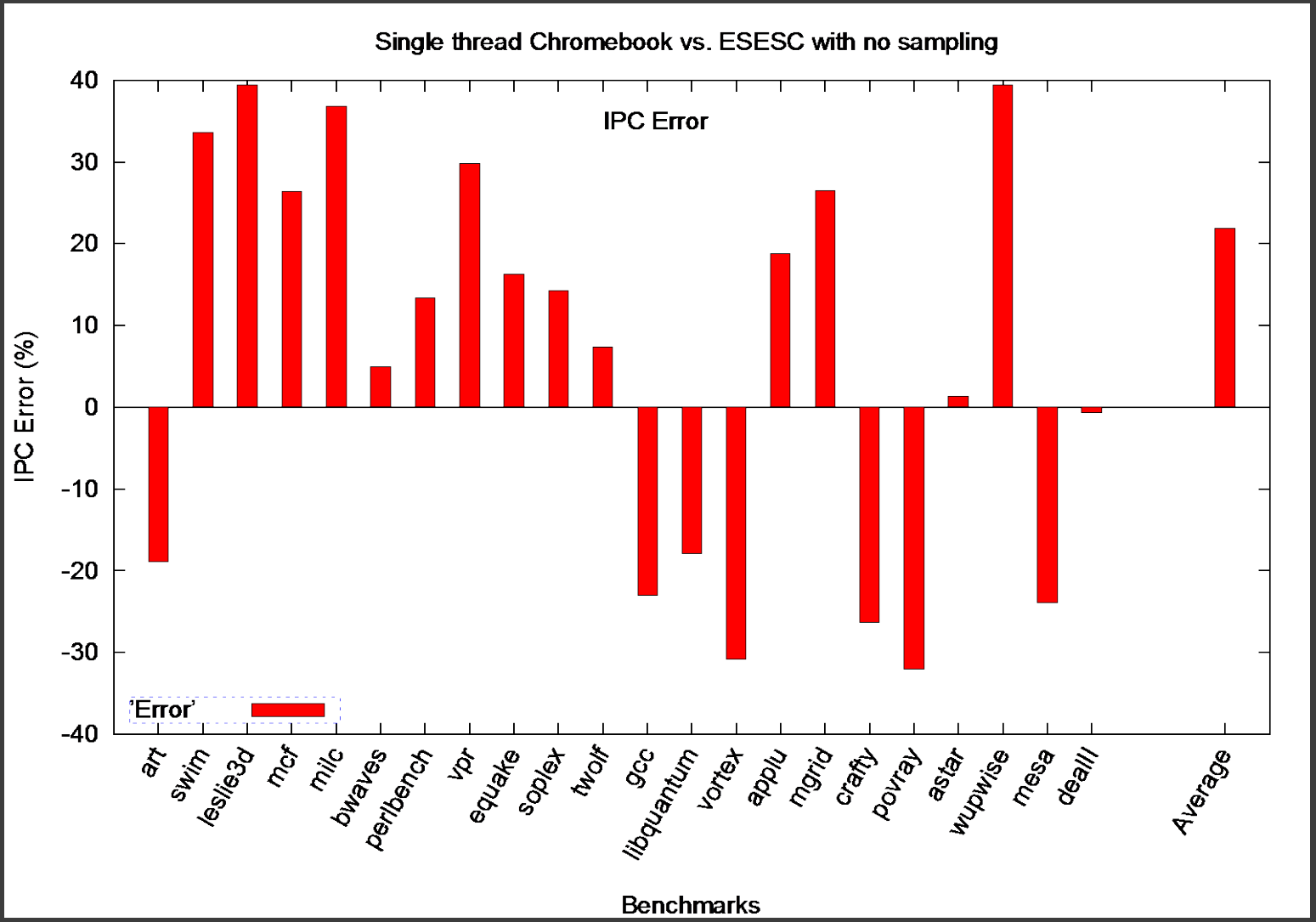

Single thread Chromebook vs. ESESC with no sampling
IPC
'Chromebook'
'ESESC'
IPC
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
art
swim
leslie3d
mcf
milc
bwaves
perlbench
vpr
equake
soplex
twolf
gcc
libquantum
vortex
applu
mgrid
crafty
povray
astar
wupwise
mesa
dealII
Benchmarks

Parameters Approximated

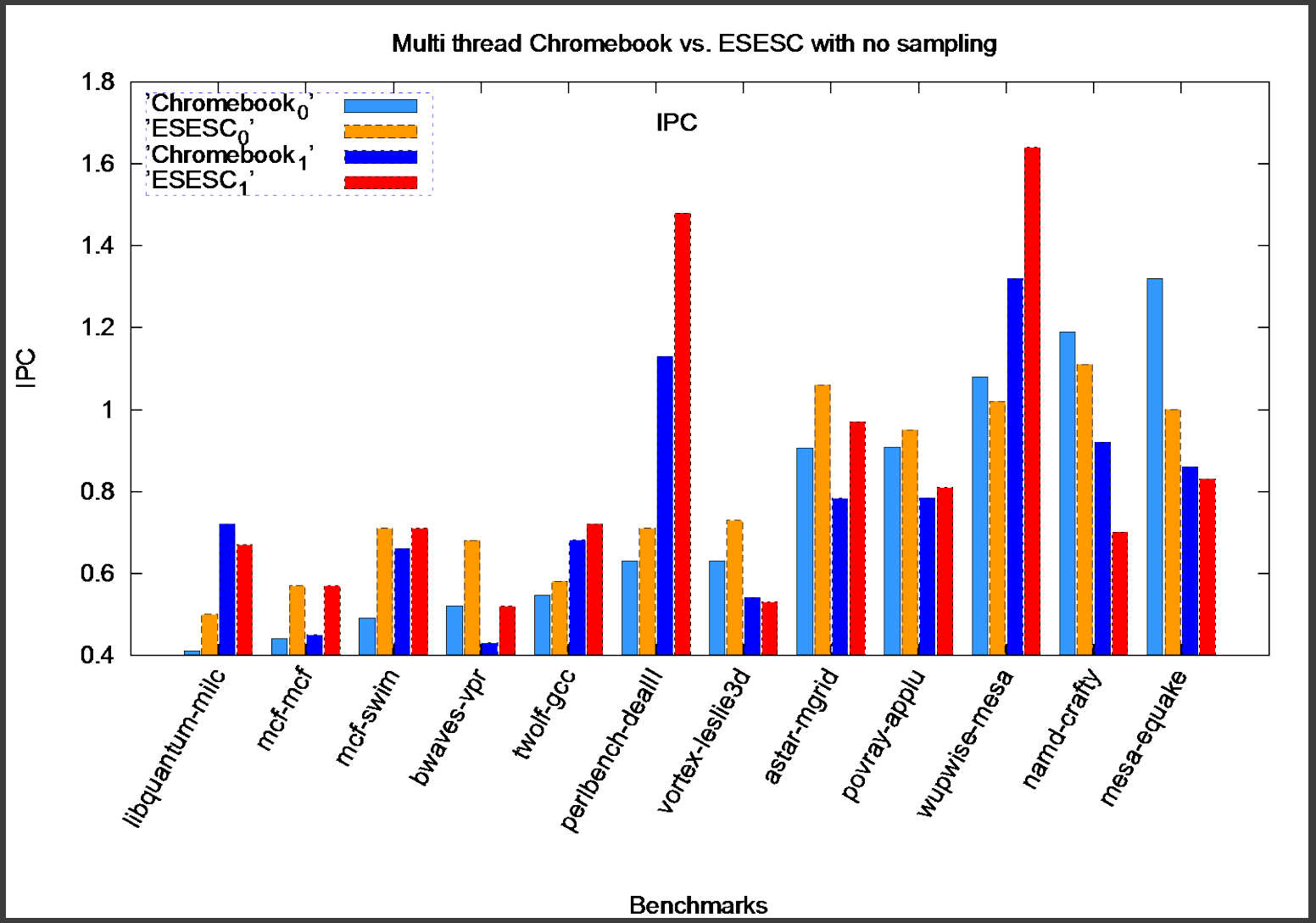
We have issues:

- No L2 pre-fetcher
- Branch predictor
  - 2 level BTB in ARM A15, but not in ESESC
- No WCB in ESESC
- Instruction Crack is not the same

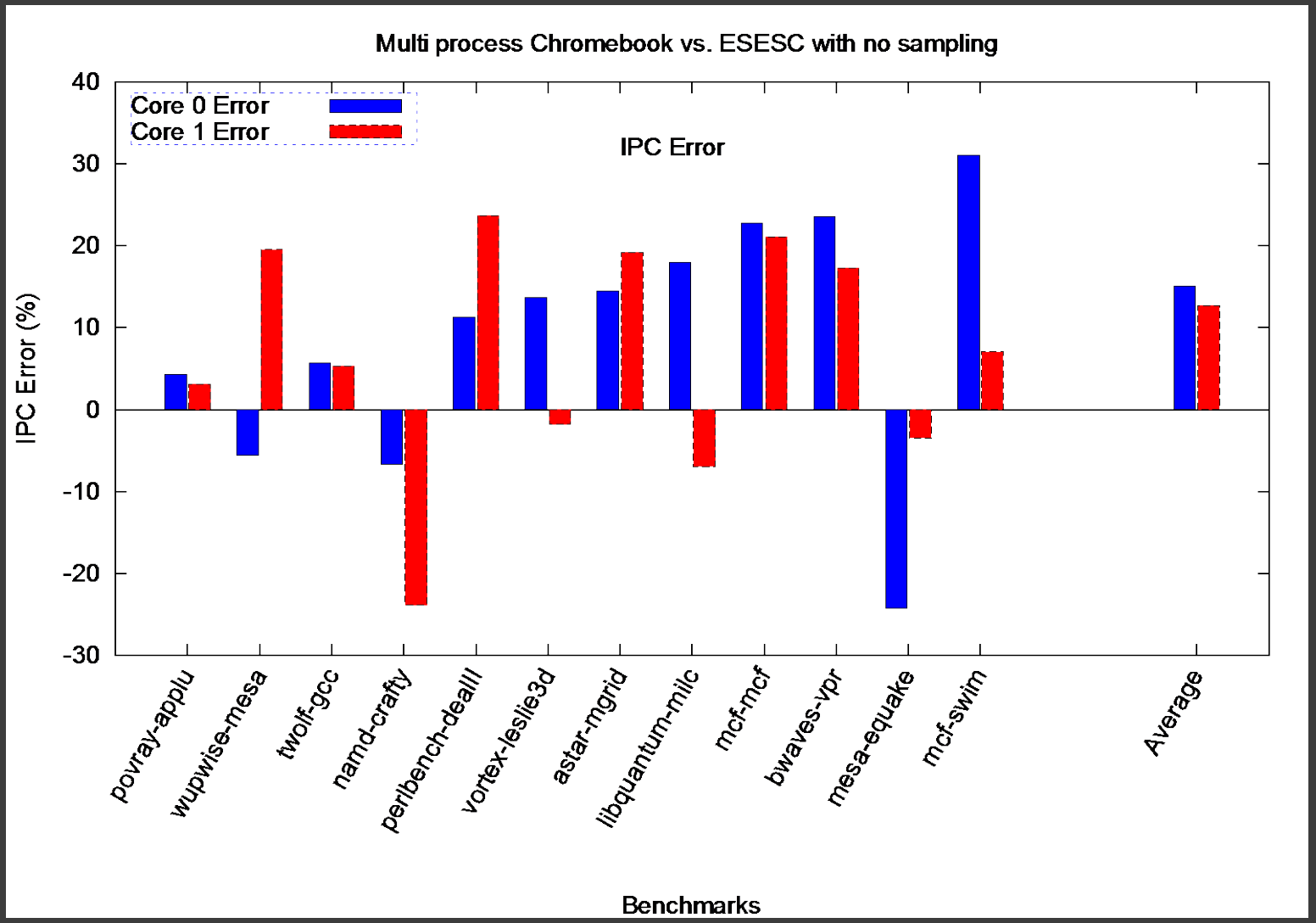
IPC Results


Single thread Chromebook vs. ESESC with no sampling
IPC Error
IPC Error (%)
40
30
20
10
0
-10
-20
-30
-40
'Error'
art
swim
leslie3d
mcf
milc
bwaves
perlbench
vpr
equake
soplex
twolf
gcc
libquantum
vortex
applu
mgrid
crafty
povray
astar
wupwise
mesa
dealII
Average
Benchmarks

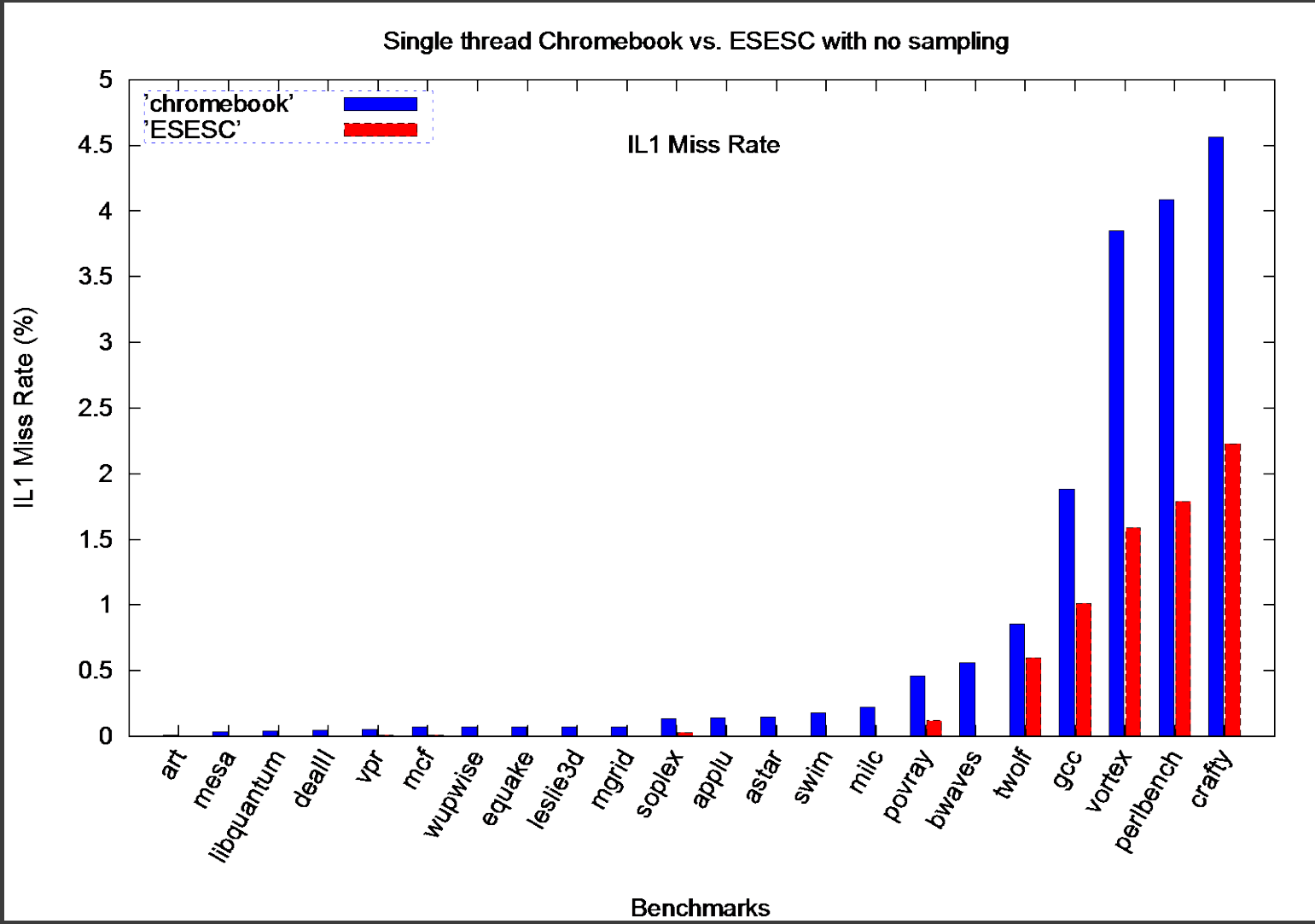
IPC Results


Multi thread Chromebook vs. ESESC with no sampling
IPC
'Chromebook0'
'ESESC0'
'Chromebook1'
'ESESC1'
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
libquantum-milc
mcf-mcf
mcf-swim
bwaves-vpr
twolf-gcc
perlbench-dealII
vortex-leslie3d
astar-mgrid
povray-applu
wupwise-mesa
namd-crafty
mesa-equake
Benchmarks

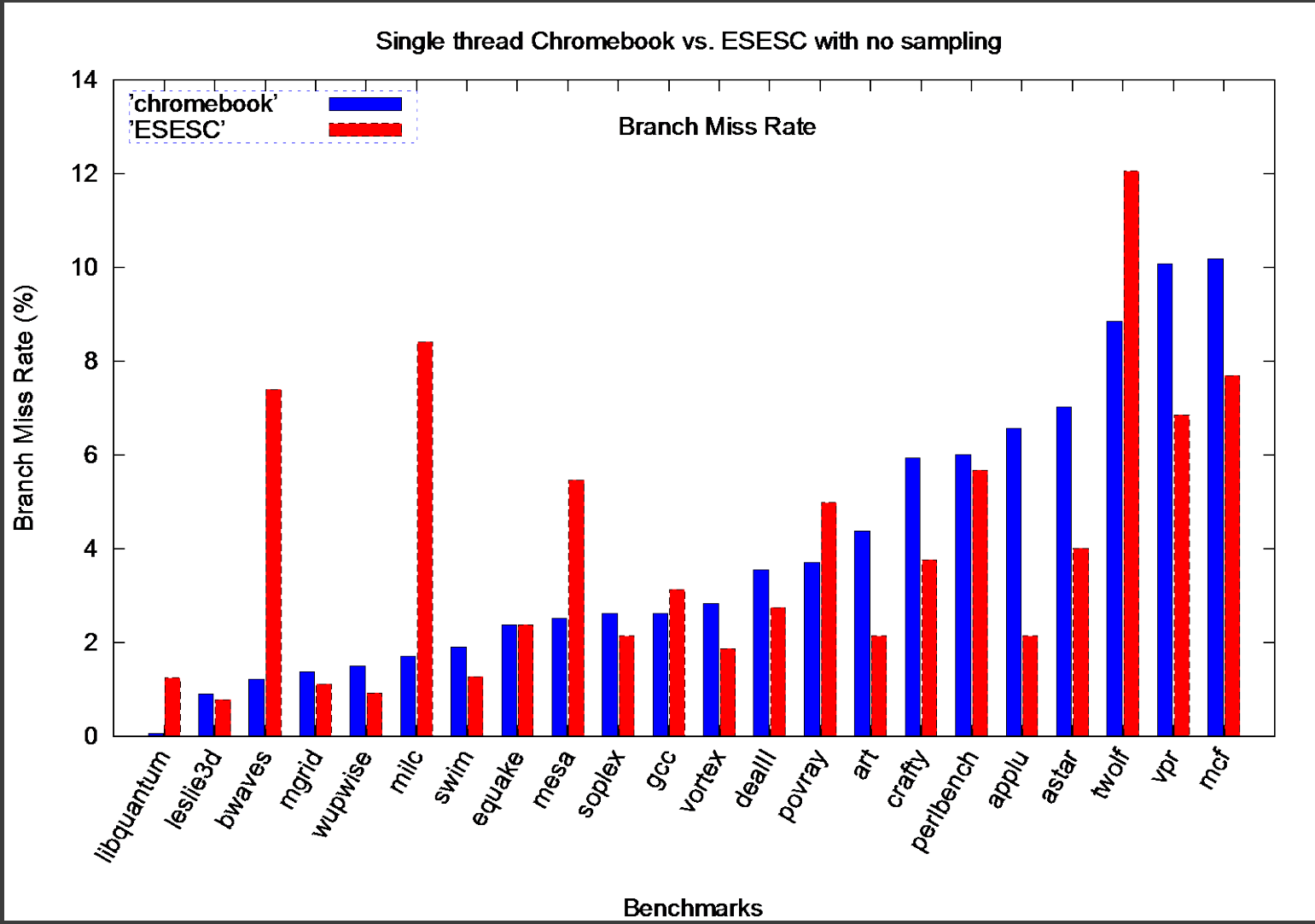
IPC Results


Multi process Chromebook vs. ESESC with no sampling
Core 0 Error
Core 1 Error
IPC Error
IPC Error (%)
40
30
20
10
0
-10
-20
-30
povray-applu
wupwise-mesa
twolf-gcc
namd-crafty
perlbench-dealII
vortex-leslie3d
astar-mgrid
libquantum-milc
mcf-mcf
bwaves-vpr
mesa-equake
mcf-swim
Average
Benchmarks

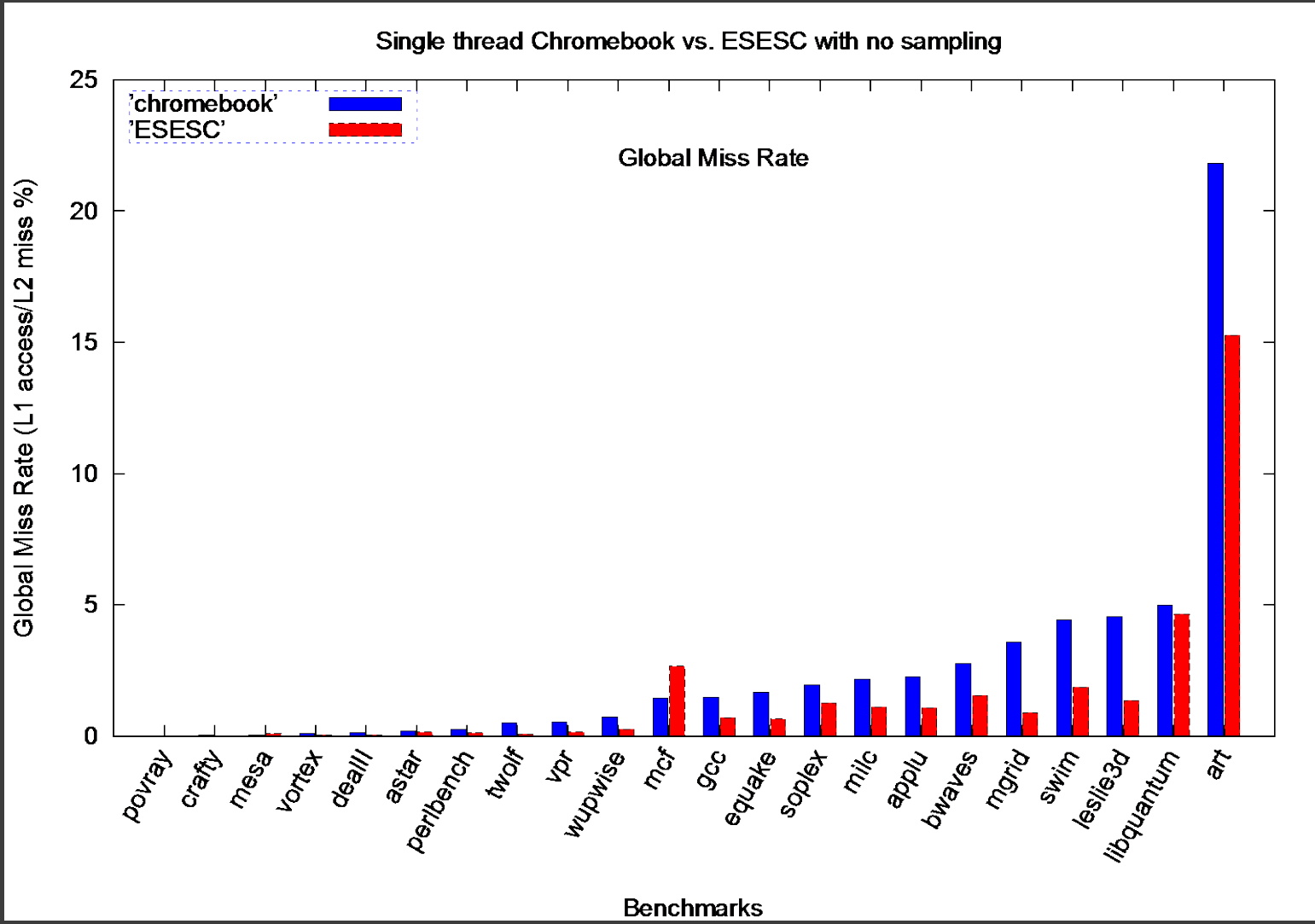
IL1 cache results



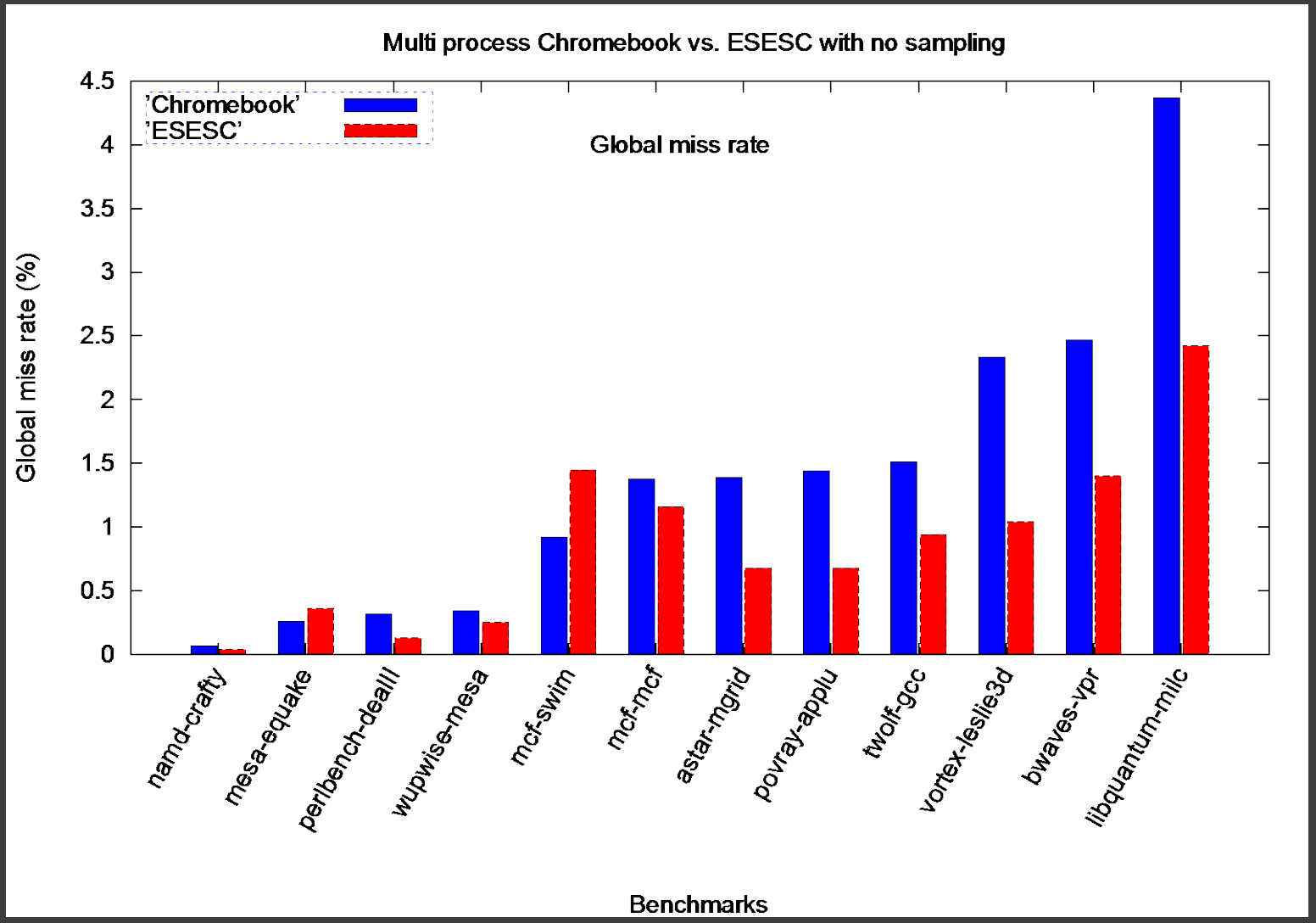
Branch predictor results



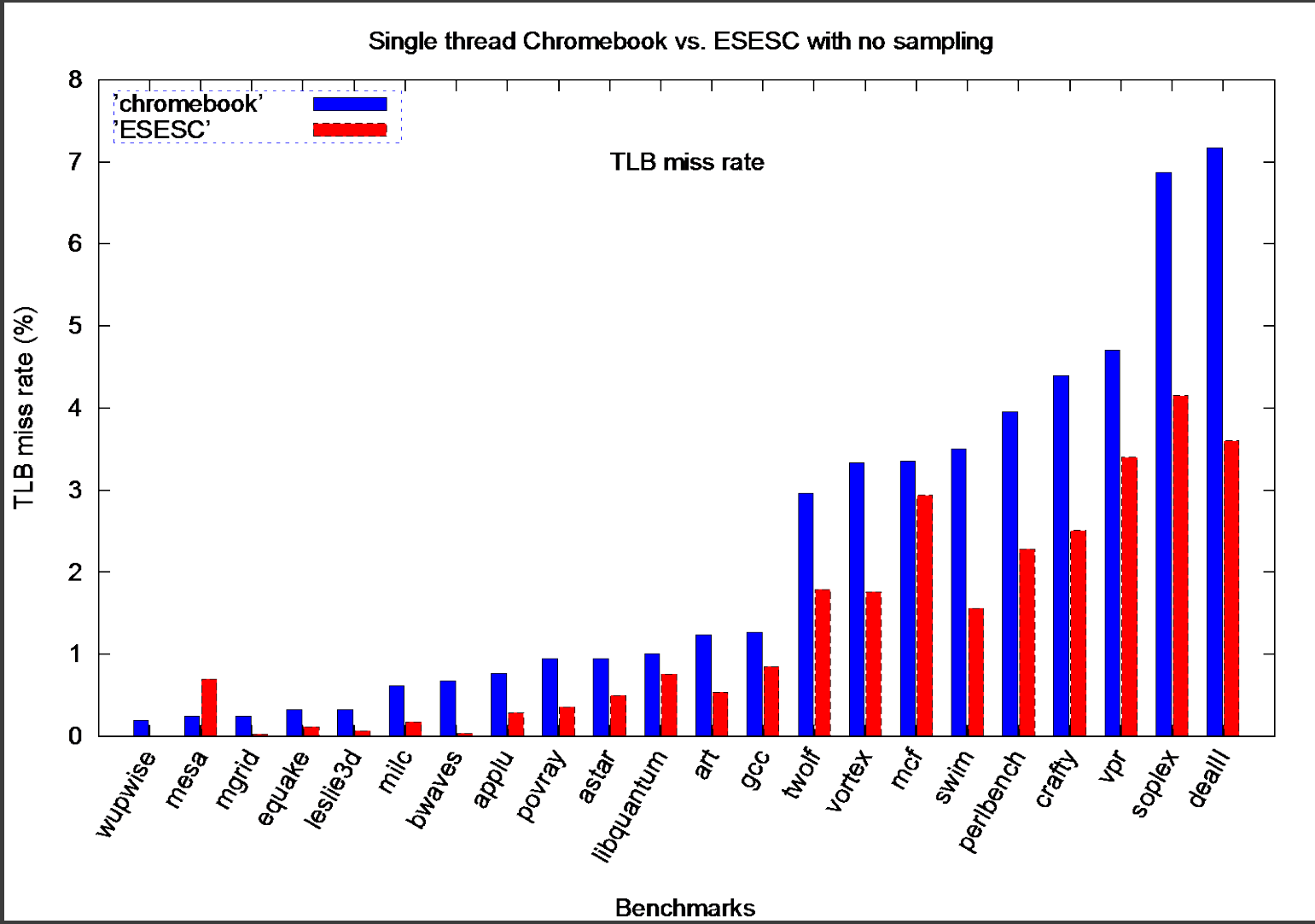
Global cache miss results



Global cache miss results



TLB miss results



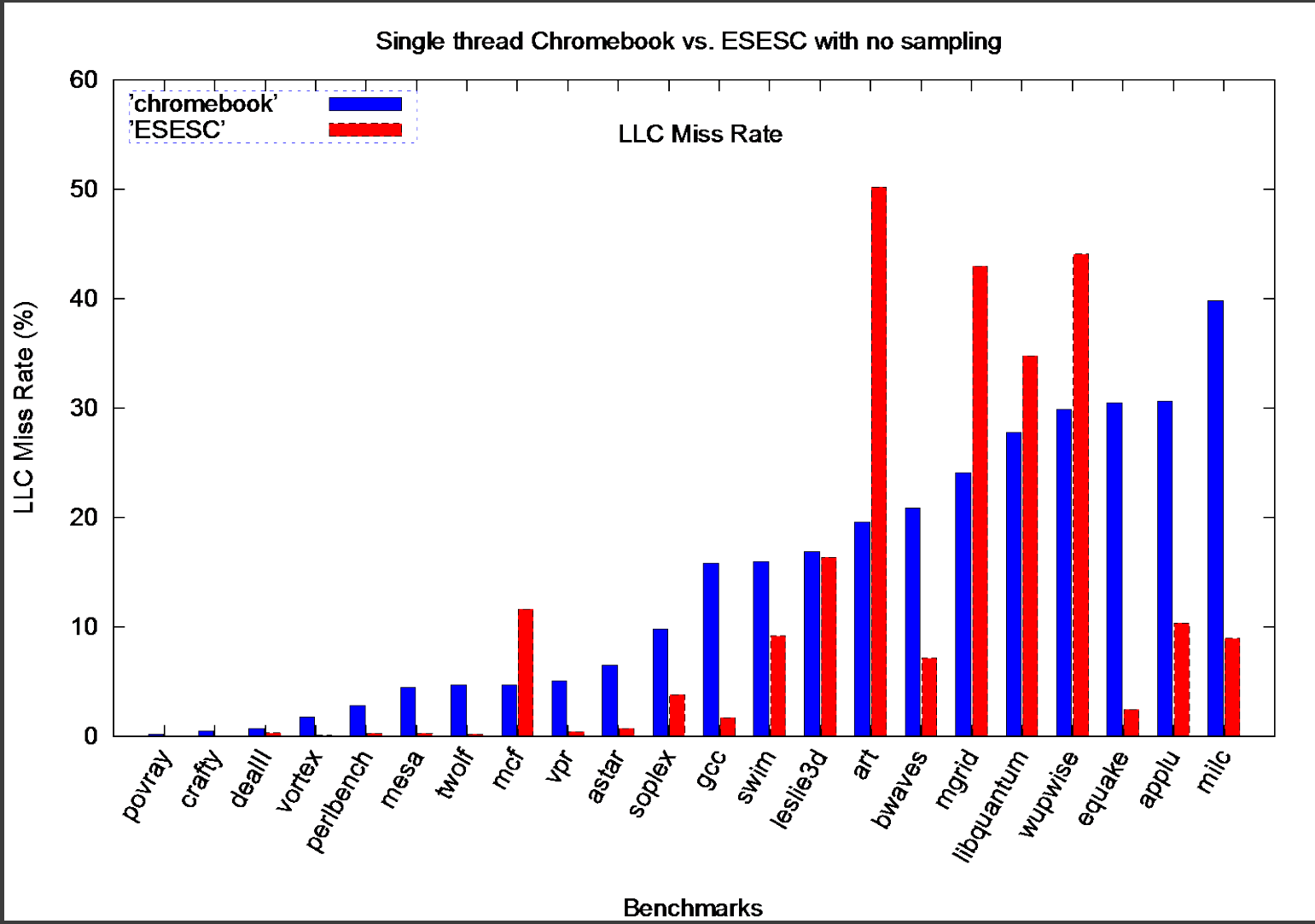
Conclusions

- ESESC is not designed to match any specific CPU
  - But it has many configuration options
- 21% average IPC error
- Quick validation of 3bil instructions

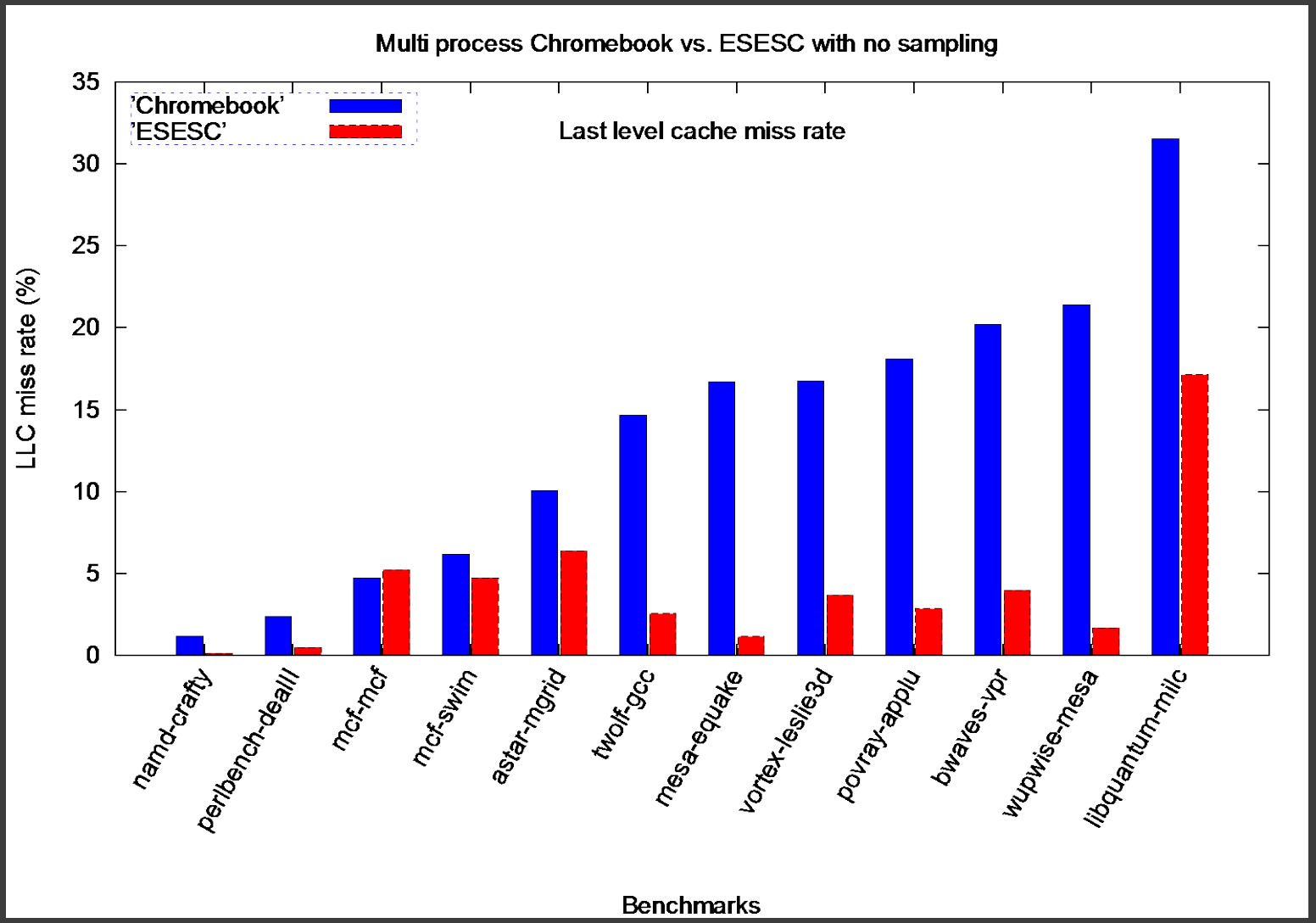
Questions?

Backup Slides

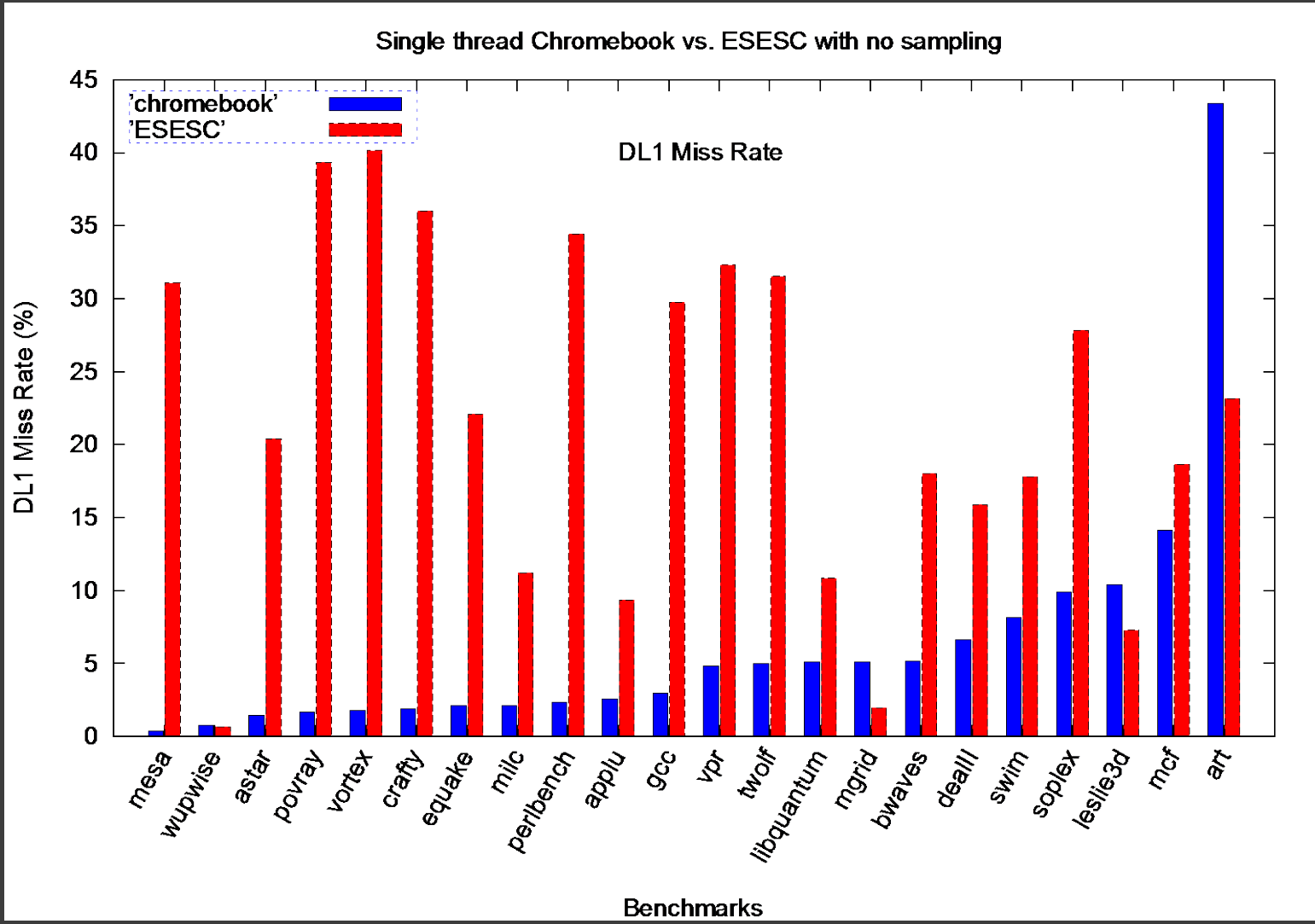
LLC results


Single thread Chromebook vs. ESESC with no sampling
'chromebook'
'ESESC'
LLC Miss Rate
LLC Miss Rate (%)
0
10
20
30
40
50
60
povray
crafty
dealII
vortex
perlbench
mesa
twolf
mcf
vpr
astar
soplex
gcc
swim
leslie3d
art
bwaves
mgrid
libquantum
wupwise
equake
applu
milc
Benchmarks

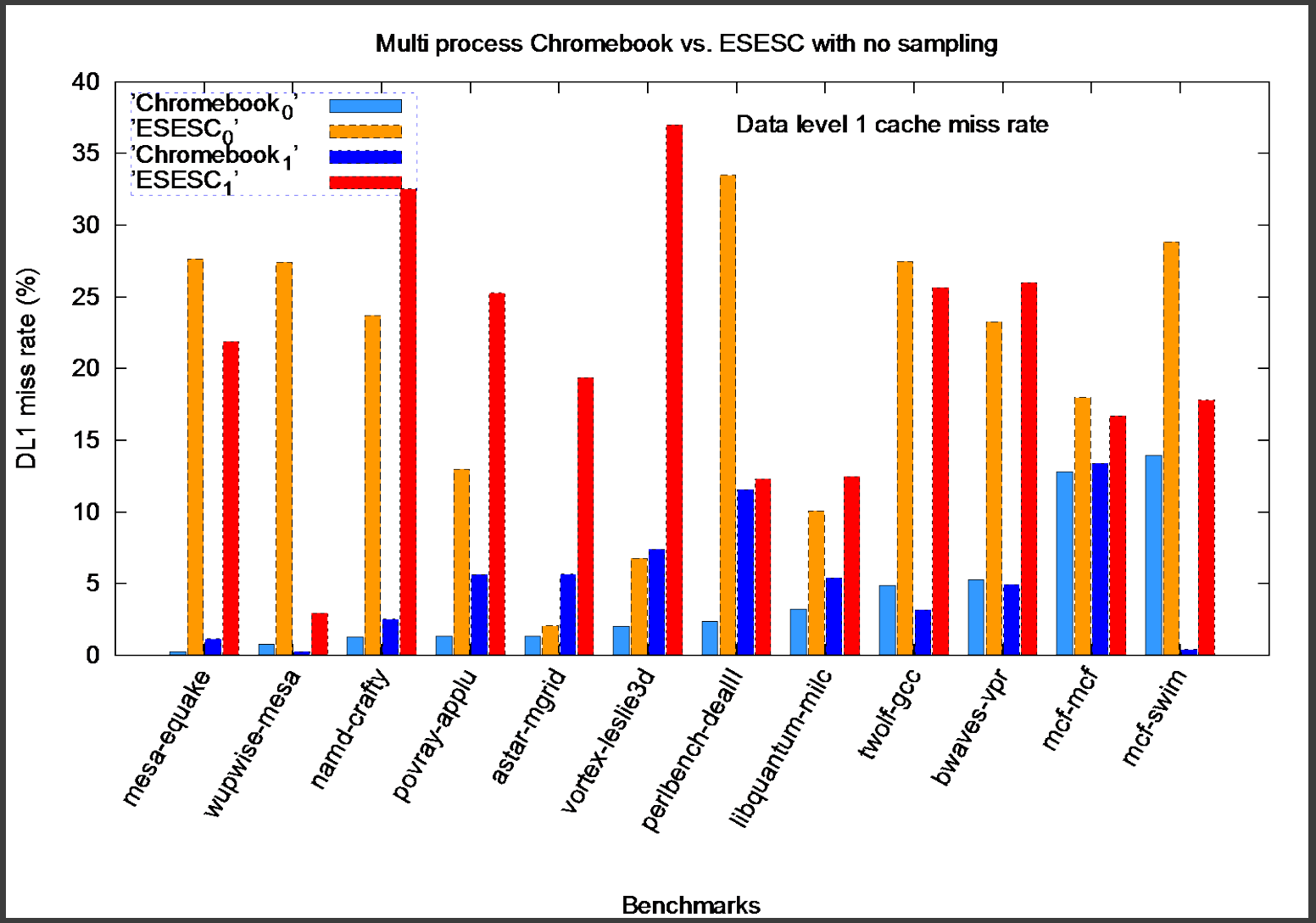
LLC results


Multi process Chromebook vs. ESESC with no sampling
'Chromebook'
'ESESC'
Last level cache miss rate
LLC miss rate (%)
0
5
10
15
20
25
30
35
namd-crafty
perlbench-dealII
mcf-mcf
mcf-swim
astar-mgrid
twolf-gcc
mesa-equake
vortex-leslie3d
povray-applu
bwaves-vpr
wupwise-mesa
libquantum-milc
Benchmarks

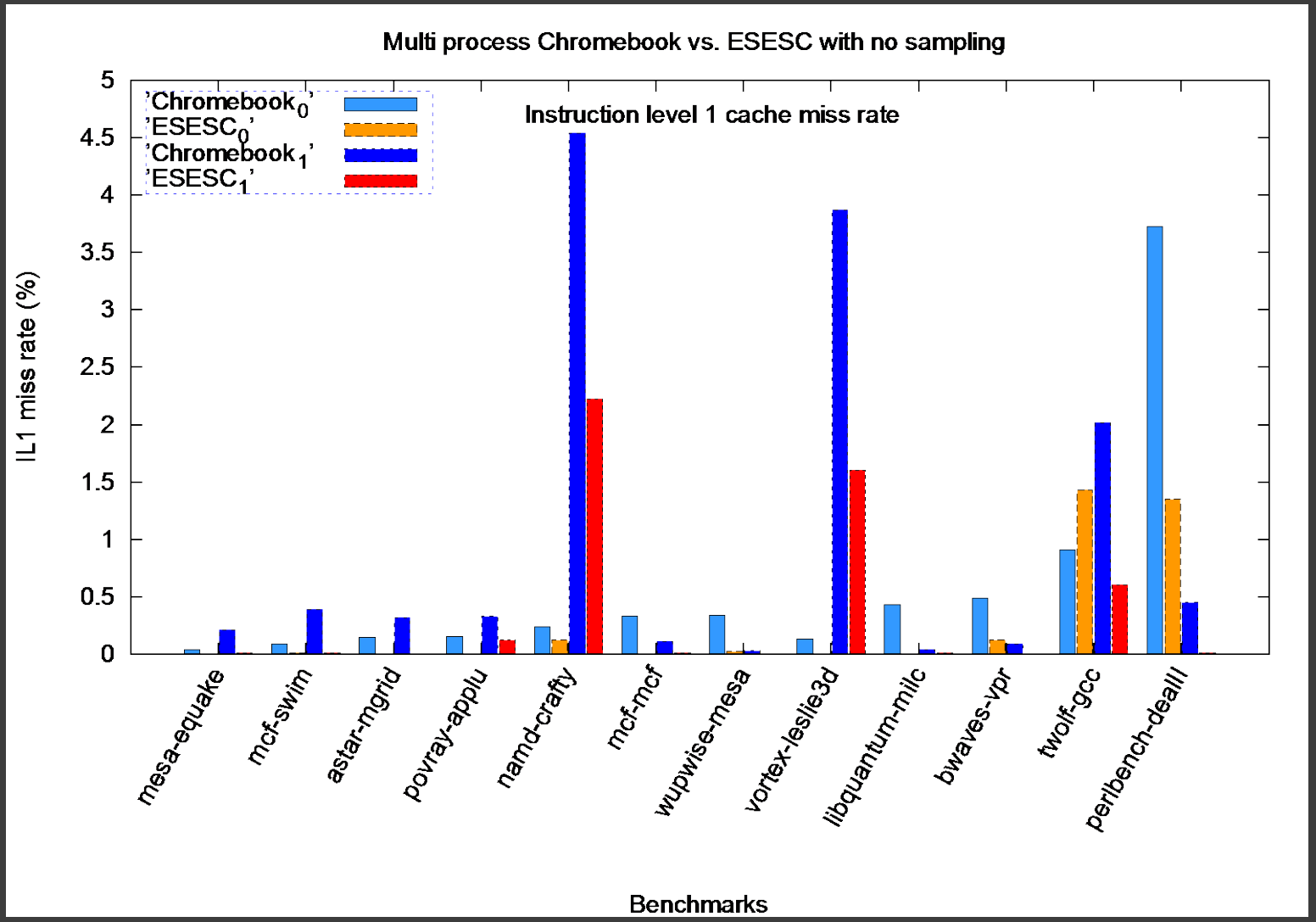
DL1 cache results



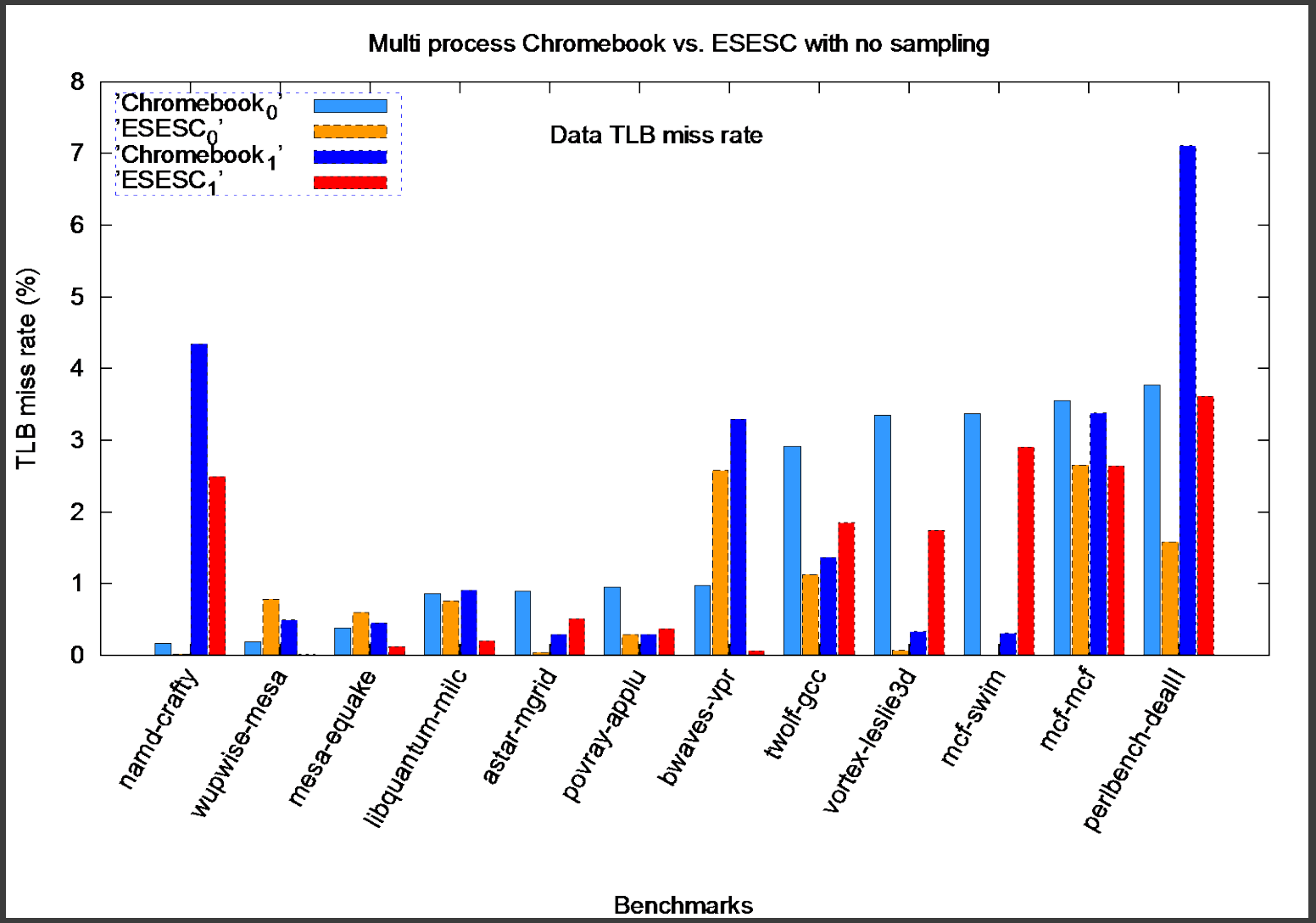
DL1 cache results



IL1 cache results



TLB miss results



Branch predictor results